DESIGN AND CHARACTERIZATION OF RF COMPONENTS FOR INTER- AND INTRA-CHIP WIRELESS COMMUNICATIONS

By

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The feasibility of implementing a high frequency tuned amplifier and integrated antennas in a CMOS technology which are needed for a wireless clock distribution system has been investigated. A wireless clock distribution system using integrated antennas has been proposed as an alternative to the conventional clock distribution network using metal interconnects. In the system, receiver and transmitter antennas replace the global clock tree and the local clock distribution from the clock receiver is accomplished through a conventional clock distribution network such as an H-tree or a grid.

A biased n-well inductor is implemented using a 0.8-μm CMOS process. Having a biased n-well reduces the parasitic capacitance between the metal spiral and substrate. It is shown that the parasitic capacitance is reduced by a factor of 2 and the quality factor is increased by 10%. A 0.6-nH inductors are implemented using a 0.1-μm CMOS process on silicon on sap-

phire (SOS) and silicon on insulator (SOI) substrates. The Q factors of the inductors are 8 and 6.5 at 12.5 GHz.

A 13-GHz tuned amplifier is implemented using a partially scaled 0.1-μm CMOS process on SOS and SOI substrates. These amplifiers are the first in a CMOS technology to have tuned frequencies greater than 10 GHz. The transducer gains are 15 dB and 5.3 dB for SOS and SOI amplifiers, respectively. The experimental results suggest that design of a ~20 GHz amplifier which is needed for the wireless clock distribution system should be possible in a fully scaled bulk 0.1-μm CMOS process.

Integrated antennas are fabricated and experimentally evaluated. Linear, meander, zigzag dipole, and loop antennas are implemented and characterized. A 2-mm long, 30-μm wide, 30-degree zigzag dipole antenna pair on a 20 Ω–cm silicon substrate shows a -56 dB gain at 18 GHz when the separation is 2 cm. A loop-zigzag pair shows -60 dB gain for a separation of 2 cm. Loop antennas with a compact size and an isotropic radiation pattern are ideal for the transmitter antenna for wireless clock distribution. Electromagnetic wave propagation of an on-chip antenna is investigated. It is shown that there are multiple wave propagation paths.

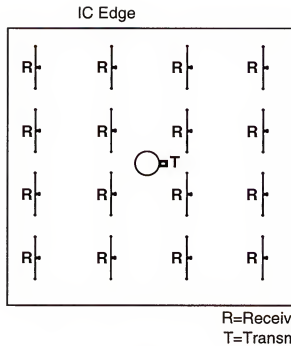
This work has shown that wireless communication within an area of 2-cm radius is feasible using integrated antennas in the absence of interference structures and opened up the possibilities of using these components to implement general purpose inter- and intra-chip wireless communication systems.

CHAPTER 1
INTRODUCTION

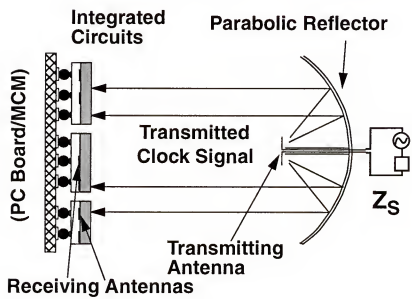
According to the International Technology Roadmap for Semiconductors (ITRS), in year 2010, the IC size will be ~2 x 4 cm^2 and the clock frequency will be ~3 GHz [IT99]. The large IC size and high clock frequency make achieving adequate clock skew challenging. Recent advances in deep sub-micron CMOS devices have enabled integration of RF front end circuits such as LNAs (low noise amplifiers), mixers, and VCOs (voltage controlled oscillators) in CMOS ICs. This has led to the introduction of the single-chip receiver concept. If the receiver circuits can be made to operate at high frequencies (~20 GHz) and such high frequency signals are used for signal transmission, antenna size can be reduced to the point where it may be possible to integrate antennas with receiver circuits on ICs. The integrated antennas and receiver circuits can be used for wireless interconnection within and between ICs using microwaves, which enables signal transmission at the speed of light. A potential application is wireless clock distribution, proposed as an alternative capable of distributing high frequency clock [O99]. Using a wireless clock distribution system can alleviate the clock skew problem because it does not suffer from the RC delays of conventional metal interconnects.

Conceptual diagrams of wireless clock distribution are shown in Figure 1-1. A wireless clock distribution system is the simplest interconnect system in terms of the signal it carries. For wireless clock distribution within a chip, a transmitting antenna can be placed in the middle of a chip, while receivers with a receiving antenna are distributed over the IC, as shown in Figure 1-1 (a). A transmitting antenna can also be placed outside of a PC board or a multi-chip module (MCM), and the ICs with receiving antennas can be placed on the PC board as shown in Figure 1-1 (b). A parabola type reflector can be used to provide electromagnetic waves with an equal phase at the surface of the PC board or MCM. Potentially, an approach like this can reduce clock skew and enable synchronization over a much larger area than ever thought possible.

A block diagram of a clock receiver is shown in Figure 1-2. In the wireless clock distribution system currently being examined, the clock signal is transmitted at ~20 GHz by the transmitter and the signal is received and frequency divided down to the actual clock frequency of ~2.5 GHz by the clock receiver. The clock receiver consists of an LNA, a frequency divider, and buffers [O99]. Since antenna efficiency is dependent on antenna size in terms of wavelengths, increasing the signal frequency to ~20 GHz reduces antenna size. The ~2.5-GHz clock signal from the output of the frequency divider is buffered and distributed to local logic circuits through a conventional clock distribution network such as an H-tree or a grid. Even though this wireless interconnection concept is being developed for clock distribution, as this tech-



(a)



(b)

Figure 1-1 Conceptual diagrams of (a) intra- and (b) inter-chip wireless clock distribution system.

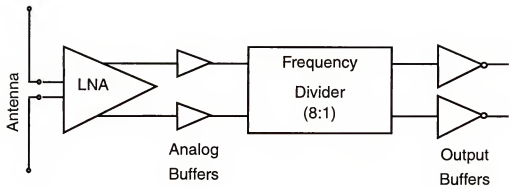


Figure 1-2 Block diagram of the receiver part of the wireless clock distribution system.

nology matures, it is expected that this concept can also be applied to general wireless interconnection or communication.

This work focuses on the development of key subcomponents for the system: integrated inductors, tuned amplifiers and integrated antennas using CMOS technologies. Use of CMOS technology is important because of its potential for low cost and ability to integrate a large system. More importantly, most of the microprocessors and logic circuits are being implemented using CMOS technologies. However, use of CMOS technology poses numerous difficulties in designing RF components due to its lossy substrates, parasitics, and low speed performance. These are challenges as well as opportunities for research.

Implementation of passive components with adequate performance is critical in RF circuit design. The performances of RF circuits are often limited by passive components rather than active devices. In tuned amplifier design, passive components, especially inductors, strongly influence the gain and noise figure. Chapter 2 presents the inductor design and characterization. The inductance computation using Grover's method, an inductor equivalent circuit model, a circuit model parameter extraction method, and Q extraction methods are described. In addition, an inductor structure with an underlying biased n-well is described [Kim97]. Having a biased n-well reduces the parasitic capacitances of the inductor. The measurement shows that the parasitic capacitance is reduced by a factor of 2 and the Q-factor is increased by ~10%. Finally, design and characterization of 0.6-nH inductors on SOI and SOS substrates for the 13-GHz tuned amplifiers described in Chapter 3 are presented. The biased n-well was not used for the 0.6-nH inductor, since the inductors were implemented on SOI and SOS substrates. The measurements show that the Q factors of the 0.6 nH inductors on SOI and SOS are monotonically increasing in the frequency range between 11 and 15 GHz. This result implies that a further optimization is required to peak the Q factors at the resonance frequency of the amplifiers. This result also implies that the inductors with Q of ~20 at 20 GHz can be easily implemented in the SOS and SOI substrates.

In Chapter 3, 13-GHz CMOS tuned amplifiers are presented. The amplifiers are the first in a CMOS technology to have tuned frequencies

greater than 10 GHz [Kim98a]. The amplifier uses a 3-stage design. The first and second stages are the gain stages using a cascode structure with an inductive load. The last stage is a common-source amplifier for buffering to a 50-Ω load. Resonance frequencies are 12 GHz and 13 GHz and gains are 5.3 dB and 15 dB for SOI and SOS amplifiers, respectively. Power consumptions are 45 mW and 58 mW for the SOI and SOS amplifiers, respectively. The power supply voltage is 1.5 V. A possible reason for the low resonance frequency and gain for the SOI amplifier compared to the SOS amplifier is presented. This result suggests that the design of a 20-GHz CMOS tuned amplifier may be possible through careful accounting of parasitics and design optimization.

Since an antenna is the largest component in a receiver, reducing antenna size is critical in implementing a wireless clock distribution system. A difficulty in reducing antenna size comes from the frequency limit imposed by CMOS technologies. Since antenna efficiency and the ability to transfer power depend on antenna size in terms of the wavelength, antenna size cannot be arbitrarily reduced. Another difficulty originates from the conductive silicon substrate, which increases loss. This reduces the antenna efficiency and also limits how small an antenna can be. For antenna characterization, especially dipole antenna characterization, baluns (balanced-to-unbalanced transformer) are needed to reduce the balanced-to-unbalanced mismatch loss [Kra88, Kaw91]. An antenna measurement set-up using a network analyzer, baluns, and signal-signal probes was developed and described in Chapter 4.

To determine the feasibility of integrated antennas on an IC, dipole and loop antennas were designed and implemented on SOI, SOS, and bulk substrates. In Chapter 5, on-chip antennas implemented on SOI, SOS, and bulk substrates are described. The resistivities of the bulk substrates are 10 and 20 Ω-cm. These substrates contained an oxide layer thickness of 1, 3, and 9 μm. Meander, zigzag, linear dipole, and loop antennas were implemented and characterized. In order to improve antenna transmission gains and optimize design, antennas with various lengths, widths, and bend angles are implemented and measured. The experimental results show that a 2-mm long, 30-μm wide, 30-degree zigzag dipole antenna pair on a 20 Ω-cm substrate has the transmission gain of -56 dB for 2-cm separation. An antenna pair consisting of loop and zigzag dipole antennas shows gain similar to the zigzag dipole pair at high frequencies (>17 GHz). Loop antennas with isotropic radiation patterns and compact sizes are ideal for transmitter applications. Antennas on SOS substrates show higher gain than on the other substrates due to lower conduction loss. This work has shown that small integrated antennas can be implemented in a chip and used for wireless interconnection within an area around a radius of 2 cm in the absence of interference structures.

The integration of antennas in silicon ICs for intra- and inter-chip communications and clock distribution has never done before. Previously, board level integration of antennas have been attempted using printed antennas on PC board [Yu92] and the integration of an antenna in an GaAs IC has been studied using microstrip antennas [Kal99]. However, the GaAs

substrate is expensive and usually not available in silicon IC technology. This work has shown that the integrated antennas can be used for short distance (~2 cm) communication even in a lossy substrate for the first time.

The propagation of electromagnetic waves from an on-chip antenna is discussed in Chapter 6. It is shown that there can be as many as three main wave propagation paths. The losses and phase delays associated with each path are studied using the plane wave assumption. The measurements using on-chip antennas on glass slides on a metal plate show interference effects. The interference effects can be explained by using two plane waves with different phase velocities and paths.

CHAPTER 2
INDUCTOR

2.1 Introduction

An inductor is a necessary component for RF blocks such as a low noise amplifier (LNA), a voltage controlled oscillator (VCO), and matching networks. Therefore, design of an inductor with an adequate quality factor (Q) using a silicon technology is important for implementing receiver circuits and matching networks for a wireless clock distribution system. Standard silicon technology imposes constraints in integration of inductors with adequate Q due to a limited number and conductivity of metal layers, substrate loss through capacitive coupling, and limited area [Ngu90]. Some non-standard practices have been attempted to overcome these constraints and to achieve high-Q inductors. However, they are expensive and hard to implement [Cha93, Bur95].

In a given process technology, the number of metal layers and the conductivity of the metal lines are fixed. Therefore, the improvement of Q by reducing loss through the metal structure is very difficult or almost impossible in a given technology. However, the improvement of Q is possible by reducing substrate loss through reducing parasitic coupling to the substrate or changing substrate resistance. The substrate resistance should be either

very high or very low to lower the substrate loss. Since achieving high resistance substrate in silicon ICs is difficult, lowering the substrate resistance is preferred to improve Q. Lower substrate resistance for an inductor can be easily obtained by using a pattern ground shield [Ton98, Yue98]. Another way to reduce the substrate loss is reducing capacitive coupling to the substrate. In this chapter, a biased n-well inductor is proposed to reduce parasitic capacitance and improve Q. This chapter also describes 0.6 nH inductors implemented on SOI (Silicon on Insulator) and SOS (Silicon on Sapphire) substrates.

2.2 Inductance Computation

2.2.1 Fundamental Definition of Inductance

Faraday and Henry found the induction of electromotive force from changing magnetic flux in the nineteenth century [Wan86, Rei79]. Their work was the basis for the development of generators, transformers, inductors, etc.

If there is magnetic induction $\overline{B}$, then the magnetic flux Φ linked to the surface S enclosed by a closed conductor wire C is defined by

$$\Phi = \int_S \overline{B} \bullet \overline{da} \tag{2.1}$$

If the direction of the closed wire is arbitrarily set, the direction of the surface is set by the right-hand rule. The vector potential $\overline{A}$ is defined by

$$\overline{B} = \nabla \times \overline{A} \tag{2.2}$$

From equation (2.2), it can be shown that

$$\overline{A} = \frac{\mu_0}{4\pi} \oint_C \frac{I\overline{ds'}}{R} \tag{2.3}$$

Where μ_0 is the permeability of free space, R represents the distance between the field point and the source point, and I is the current in the conductor wire C. Using the vector potential $\overline{A}$, Φ can be written as

$$\Phi = \int_S \overline{B} \bullet \overline{da} = \oint_C \overline{A} \bullet \overline{ds} = \oint_C \frac{\mu_0}{4\pi} \oint_C \frac{I'\overline{ds'}}{R} \bullet \overline{ds} \tag{2.4}$$

For two closed conductor wires C_j and C_k as shown in Figure 2-1 and the magnetic flux linked to C_j from C_k can be expressed as

$$\Phi_{j \to k} = \oint_{C_j} \frac{\mu_0}{4\pi} \oint_{C_k} \frac{I_k \overline{ds_k}}{R_{jk}} \bullet \overline{ds_j} \tag{2.5}$$

using equation (2.4).

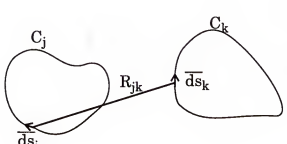


Figure 2-1 Positions of two line elements on two closed wire to calculate mutual inductance.

Since I_k is a scalar quantity, mutual inductance can be defined from equation (2.5) as

$$\Phi_{jk} = M_{jk} I_k \tag{2.6}$$

$$M_{jk} = \frac{\mu_0}{4\pi} \oint_{C_j} \oint_{C_k} \frac{\overline{ds_j} \bullet \overline{ds_k}}{R_{jk}} \tag{2.7}$$

Equation (2.7) shows that the mutual inductance is a purely geometrical factor relating the size and relative orientation of the two elements. The calculation of the magnetic flux linked to C_k from C_j shows that $M_{kj}=M_{jk}$. It is also observed that the contribution of two perpendicular line elements to the mutual inductance is zero, since for this case $\overline{ds_j} \bullet \overline{ds_k} = 0$.

Self-inductance can be obtained by calculating the magnetic flux linked to itself.

$$\Phi_{j \to j} = L_{jj} I_j = \oint_{C_j} \frac{\mu_0}{4\pi} \oint_{C_j} \frac{\overline{ds_j}}{R_{jj}} \bullet \overline{ds_j} I_j \tag{2.8}$$

This equation shows that the self inductance is always positive.

If the magnetic flux linked to a loop C is changing with time, then it will induce current in the loop C. Since the induced current depends on the resistance of the loop C, it is more convenient to use induced emf or electromotive force to express the effect of the changing magnetic flux. It is found that

$$\varepsilon_{ind} = -\frac{d\Phi}{dt} = -L\frac{dI}{dt} \tag{2.9}$$

The minus sign in equation (2.9) represents the direction of the emf compared to the original arbitrarily chosen direction of C. The direction is governed by Lenz' law: "The induced emf has such a sense as to oppose the change that is producing it". As mentioned earlier, if there is a time varying magnetic field and a conductor, then eddy current will be generated in the conductor. As it is predicted by the Lenz' law, the direction of eddy current is always to oppose the change of magnetic field. Therefore, the eddy current reduces the magnetic energy storage in the system. In addition, the flow of eddy current in the conductor generates ohmic loss, which increases the energy loss.

2.2.2 Grover's Method

The inductance computation method for an on-chip spiral inductor is well established and proven to be accurate [Gro46, Gre74]. The FastHenry simulator has been used for inductance computation in this work. It uses Grover's method [Kam93].

Grover's method can compute inductances of any 3D inductor. Inductor structures do not have to be planar, but they should consist of straight line segments in Grover's method. In order to compute inductances using Grover's method, an inductor structure should be divided into straight line segments as shown in Figure 2-2. The total inductance of the inductor can be obtained by computing the self-inductance of each segment and the mutual induc-

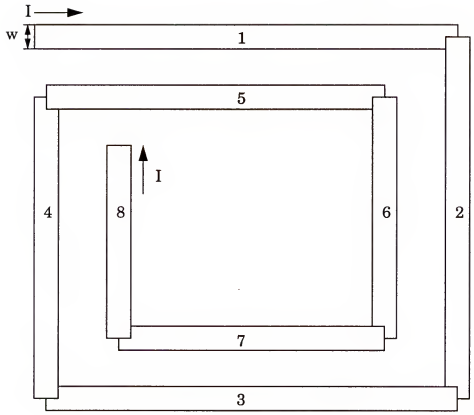


Figure 2-2 Segmentation of a spiral inductor for inductance computation using FastHenry.

tances between each pair of segments. The total inductance is the sum of all the self and mutual inductances.

Self-inductance of a metal line segment with a rectangular cross section is computed using equation (2.10) for the near direct current case [Gre74]. The near direct current case implies that the length of the line segment is small enough compared to the wavelength so that the phase of the current flowing in the line segment essentially does not change.

$$L = 0.002l\left\{\ln\left[\frac{2l}{(a+b)}\right] + 0.50049 + \frac{(a+b)}{3l}\right\} \tag{2.10}$$

where l is the length of the metal line segment in centimeters and a and b are the width and thickness of the metal line in centimeters. L is the inductance in microhenries. Mutual inductance in microhenries between two equal length parallel metal line segments is computed using the following equation,

$$M = 0.002l\left[\ln\left\{\frac{l}{GMD} + \sqrt{1 + \frac{l^2}{GMD^2}}\right\} - \sqrt{1 + \frac{l^2}{GMD^2}} + \frac{GMD}{l}\right] \tag{2.11}$$

where l is the length of the metal line segments in centimeters and *GMD* is the geometric mean distance between the two parallel lines, which is approximately equal to the distance d between the centers of the line segments. The exact value of the *GMD* between two metal lines with equal width and thickness can be calculated from the following equation,

$$\ln(GMD) = \ln(d) - \left\{\frac{1}{12}\left(\frac{w}{d}\right)^2 + \frac{1}{60}\left(\frac{w}{d}\right)^4 + \frac{1}{168}\left(\frac{w}{d}\right)^6 + \frac{1}{360}\left(\frac{w}{d}\right)^8 + \frac{1}{660}\left(\frac{w}{d}\right)^{10} + \ldots\right\} \tag{2.12}$$

where w is the width of the metal line segments. For two unequal-length parallel metal line segments shown in Figure 2-3, mutual inductance ($M_{j,m}$) can be calculated using the following equation.

$$2M_{j,m} = M_{m+p} + M_{m+q} - (M_p + M_q) \tag{2.13}$$

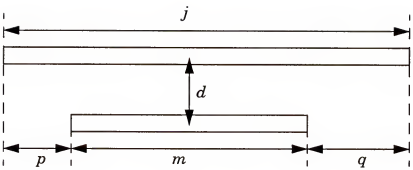


Figure 2-3 Two unequal-length parallel line segments.

M_{m+p} is the mutual inductance between two parallel line segments of a length $m+p$ with a distance d, M_{m+q} is that for a length m+q, M_p is for a length p, and M_q is for a length q.

In order to calculate the total inductance of the spiral inductor, as mentioned, self inductances of each straight line segment using equation (2.10) and mutual inductances between each pair using equations (2.11) and (2.13) should be calculated and added. The inductance of the spiral inductor shown in Figure 2-2 is

$$L_T = L_1 + L_2 + L_3 + L_4 + L_5 + L_6 + L_7 + L_8 + 2(M_{1,5} + M_{2,6} + M_{3,7} + M_{4,8})$$

$$-2(M_{1,7} + M_{1,3} + M_{5,7} + M_{5,3} + M_{2,8} + M_{2,4} + M_{6,8} + M_{6,4}). \qquad (2.14)$$

Mutual inductance is zero when two straight conductors are perpendicular. When current flows in two parallel conductors are in the opposite direction,

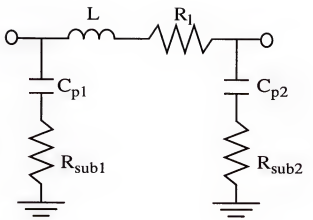
mutual inductance is negative and when they are in the same direction, mutual inductance is positive. As mentioned earlier, inductances of any 3-D structures can be calculated using this procedure.

2.3 Equivalent Circuit Model and Parameter Extraction

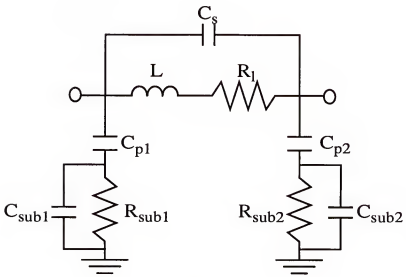
2.3.1 An Inductor Equivalent Circuit Model

Equivalent lumped element circuit models for on-chip spiral inductor structures are used to predict the circuit performance using SPICE when spiral inductors are included in a circuit. The lumped element model parameters are extracted from measurements. It is difficult to accurately model spiral inductors using lumped elements due to the distributed nature of the spiral inductor. This is one of the reasons why the extracted values of the lumped elements from measurements usually show frequency dependence [Lon95]. The model parameters are also temperature dependent [Gro97].

Figure 2-4 shows two widely used inductor lumped element models. Figure 2-4 (a) shows the basic π model which was verified using measurements and 3-D EM simulations [Ngu90, Cro96]. In this model, R_l represents the metal series resistance, C_{p1} and C_{p2} represent parasitic capacitance between metal lines and the substrate, and R_{sub1} and R_{sub2} represent substrate resistances. This model is the simplest and it is easy to extract all the model parameters from s-parameter measurements of inductors as will be discussed in section 2.3.2. A disadvantage of this model is the fact that the



(a)



(b)

Figure 2-4 Two equivalent lumped element circuit models for the on-chip inductor.

model parameters have frequency dependencies. The frequency dependencies of the model parameters come from skin effect [Smi98], proximity effect [Gle72, Lot92], eddy current, as well as the distributed nature of the on-chip inductor [Cro96]. The skin effect and proximity effect increase R_l at high frequencies and the eddy current reduces L and increases R_l especially when the conductivity of a silicon substrate is high. The distributed nature of an on-chip inductor greatly affects both R_l and L at the frequencies near the self-resonance of an inductor. The model parameters R_l, L and C_p can be predicted from the geometry. The prediction of R_{sub} requires 3-D EM simulations or measurements. The inductor model in Figure 2-4(b) has been also suggested and utilized [Ash96, Nik97, Yue96]. It is claimed that this model is more physically based. The basic model parameters are the same as the model in Figure 2-4(a) but substrate parasitic capacitances (C_{sub}) and parasitic capacitance between metal lines (C_s) are added. R_{sub} and C_{sub} are proportional to the area covered by the spiral inductor. The prediction of these values requires 3-D EM simulation or extraction from measured data using a curve fitting technique. The majority of C_s comes from the parasitic capacitance between the spiral and center-tap underpass. This capacitance is usually less than 10% of C_p and can be ignored. Even though the model shown in Figure 2-4(b) is more complicated than that in (a), its model parameters are still frequency dependent.

Since it is more convenient to extract and predict model parameters using the model in Figure 2-4(a), and this model has been shown to model on-chip spiral inductor reasonably well, this model has been used in this work.

2.3.2 Parameter Extraction Method

The model parameters can be extracted from the measured S-parameters of an inductor. In order to extract the model parameters, S-parameters should be converted to Y-parameters and the model parameters can be obtained using the following formula.

$$L = \text{imag}\left(\frac{-1}{\omega Y_{21}}\right) \tag{2.15}$$

$$R_l = \text{real}\left(\frac{-1}{Y_{21}}\right) \tag{2.16}$$

$$C_{p1} = \frac{-\text{imag}(Y_{11} + Y_{21})}{\omega} \tag{2.17}$$

$$R_{sub1} = \text{real}\left(\frac{1}{Y_{11} + Y_{21}}\right) \tag{2.18}$$

C_{p2} and R_{sub2} can be obtained by replacing Y_{11} to Y_{22} in equations (2.17) and (2.18), respectively. An inductor test structure usually includes input and output pads. These pads add extra parasitic capacitances. These parasitic capacitances decrease the extracted Q-factor and increase the extracted values of C_{p1} and C_{p2}. To de-embed the parasitic capacitances of the pads, it is necessary to measure the S-parameters of a test structure with open pads. The S-parameters of the open pads should be converted to Y-parameters and

the Y-parameters of the open pads should be subtracted from the Y-parameters of the inductor test structure. The model parameters should be extracted after the subtraction.

2.4 Quality Factor

2.4.1 Fundamental Definition of Quality Factor

Quality factor (Q) is a dimensionless number. It is defined for a resonant circuit and provides a measure of sharpness of a resonance response or loss in a resonant circuit. Lower loss implies higher Q [Kaj94, Jac75]. The definition of Q is the same for both lumped-element resonant circuits and microwave distributed resonators. It is expressed as an energy ratio [Col66].

$$Q = 2\pi\left[\frac{W_{max}}{W_d}\right]_{\omega = \omega_0} \tag{2.19}$$

W_{max} is the maximum energy stored in the resonator. When the electromagnetic field in the resonator is varying, it is the peak value of the stored energy. W_d is the dissipated energy during one period. The ratio must be evaluated at the resonance frequency. A period of the oscillation is $T = \frac{2\pi}{\omega}$. The energy loss in one period is $W_d = TP_d$, where P_d is the average power dissipation. Thus, Q can be expressed as

$$Q = \omega\left[\frac{W_{max}}{P_d}\right]_{\omega = \omega_0}. \tag{2.20}$$

In a simple RLC resonant circuit, the peak magnetic energy storage is generally different from the peak electric energy storage. However, at the resonance frequency, the peak energy storages are equal. Since the average energy values are equal to one half of their peak values, the maximum stored energy is

$$W_{max} = W_m + W_e . \tag{2.21}$$

Using the above equation, Q can be written as

$$Q = \left[\frac{2\omega W_e}{P_d}\right]_{\omega=\omega_0} = \left[\frac{2\omega W_m}{P_d}\right]_{\omega=\omega_0} = \omega\left[\frac{W_m + W_e}{P_d}\right]_{\omega=\omega_0} \tag{2.22}$$

W_e and W_m are the average electric and magnetic energy.

For simple RLC resonant circuits, Q can be related to the 3-dB band widths of the circuit's resonance response [Des69, O98a].

$$Q = \frac{\omega_0}{\Delta\omega} \tag{2.23}$$

ω_0 is the resonance frequency and $\Delta\omega$ is the 3-dB band width.

2.4.2 Conventional Q-Extraction Method

The quality factor calculation method typically used to extract Q of an on-chip spiral inductor is referred as Q_{conv} and defined as follows [O98a, Yue98].

$$Q_{conv} = -\frac{Imag(Y_{11})}{Real(Y_{11})} = \frac{2\omega(|\overline{W_m}| - |\overline{W_e}|)}{P_{diss}} \tag{2.24}$$

$|\overline{W_m}|$ and $|\overline{W_e}|$ are the average stored magnetic energy and electric energy in a spiral inductor structure. P_{diss} is the average power dissipation. This Q definition involves a subtraction of the electric energy storage from the magnetic energy storage rather than the sum of those two as in equation (2.22). When the magnetic energy storage is much greater than the electric energy storage, the Q calculation using equation (2.24) is close to the Q from equation (2.22). However, when the electric energy storage is close to the magnetic energy storage, Q_{conv} can become very small, and when the former is greater than the latter, Q_{conv} would become negative. In fact, the fundamental definition of Q in section 2.4.1 tells us that Q cannot be negative. Therefore, the calculation of Q using equation (2.24) can give unreasonable Q estimations when the two type of energy storages are comparable or the electric energy storage is greater than the magnetic energy storage.

For an on-chip spiral inductor, when port 2 is grounded, it can be treated as an RLC parallel resonant circuit as shown in Figure 2-5 by converting the series elements to parallel elements. The average stored electric and magnetic energy and the power dissipation can be expressed as

$$|\overline{W_e}| = \frac{V^2}{4C} \tag{2.25}$$

$$|\overline{W_m}| = \frac{1}{4}LI^2 = \frac{V^2}{4\omega^2 L} \tag{2.26}$$

$$P_{diss} = \frac{V^2}{2R}. \tag{2.27}$$

V is the amplitude of the sinusoidal input voltage. Using equation (2.24), Q_{conv} is

$$Q_{conv} = \frac{R}{\omega L}\left(1 - \left(\frac{\omega}{\omega_0}\right)^2\right) \tag{2.28}$$

where ω_0 is the resonance frequency, which is

$$\omega_0 \cong \frac{1}{\sqrt{LC}} \tag{2.29}$$

The equation (2.28) implies that when the frequency is low ($\omega < \omega_0$), the Q_{conv} is positive and the impedance is inductive, and when the frequency is high ($\omega > \omega_0$), the Q_{conv} is negative and the impedance is capacitive. When the frequency is equal to the self-resonance frequency, Q_{conv} is equal to zero. However the fundamental definition of Q in section 2.4.1 tells us that the Q cannot be zero or negative. In fact, Q_{conv} introduces errors when the electric energy storage becomes non-negligible at moderate to high frequencies and a

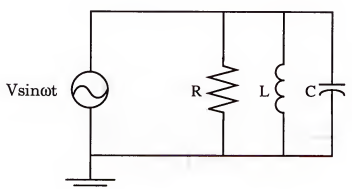


Figure 2-5 A RLC parallel resonant circuit.

new Q-extraction method is necessary to properly estimate the Q of an inductor.

2.4.3 A New Q-Extraction Method

Due to the limitations of the conventional Q extraction method described in section 2.4.2, a new Q extraction method has been proposed [O98a, Ton98]. This Q extraction method involves the band width Q definition shown in equation (2.23). The Q estimation using this definition will give a correct Q of an inductor at moderate to high frequencies. In most cases, a spiral inductor is connected to capacitors in parallel and used as a tank circuit. The capacitance can be from either parasitic capacitances of devices or from those purposely added. When the capacitance is added, the resonance frequency of the resulting circuit is lowered from the self resonance frequency of the inductor. Q of the resulting tank circuit will also be different from the Q of the inductor at its self resonance frequency.

To estimate Q of an inductor at a frequency different from the self-resonance frequency, a numerical capacitance (C_{num}) can be added to the measured input admittance data of the inductor and the band width of the total tank circuit including C_{num} can be estimated as shown in Figure 2-6. The addition of the numerical capacitance to the measured Y_{in} can be done easily by computing $Y_{tot}=Y_{in}+j\omega C_{num}$. The band width($\Delta\omega$) can be computed using $Z_{tot}=1/Y_{tot}$ and

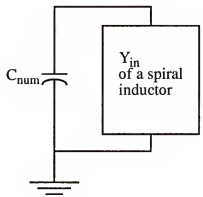


Figure 2-6 Adding a C_{num} to the Y_{in} of a spiral inductor.

$$|Z_{tot}(\omega)| = \frac{1}{\sqrt{2}}|Z_{tot}(\omega_0)|. \tag{2.30}$$

Equation (2.30) will give two frequencies (ω_1 and ω_2) and the $\Delta\omega = |\omega_2 - \omega_1|$.

By sweeping the numerical capacitance, Q of the inductor can be obtained at a range of frequencies. This computation of Q can easily be done using Matlab [Mat92]. Figure 2-7 shows abs(Z_{tot}) after adding C_{num} to the measured Y_{in}. For each value of C_{num}, ω_0 and $\Delta\omega$ can be computed. The extracted Q in this way is called Q_{BW}. The Q_{BW} represents the maximum Q which can be obtained when the inductor is used in a tank circuit, because in real circuits, the addition of capacitance always results in adding resistance. Since the addition of C_{num} will always decrease the resonance frequency, the maximum frequency for which the Q_{BW} can be computed is the self resonance frequency of an inductor.

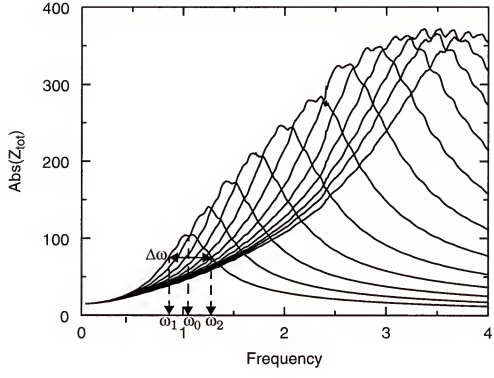
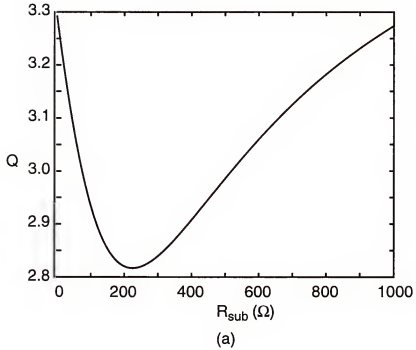


Figure 2-7 Abs(Z_{tot}) of an inductor after adding C_{num} to calculate Q_{BW}.

2.4.4 Substrate Effect on Inductor Q

As shown in Figure 2-4, an on-chip spiral inductor has parasitic capacitances and resistances. These parasitics lower Q of an inductor. Therefore, understanding of substrate parasitic effects on the inductor Q is important.

To estimate the effects of the substrate parasitics on inductor Q, the inductor model shown in Figure 2-4(a) is used and Y_{in} of the inductor was calculated using Matlab. The conventional definition of Q was used to estimate the Q for simplicity. Figure 2-8 shows Q vs. R_{sub} (a) and Q vs. C_p (b) plots.



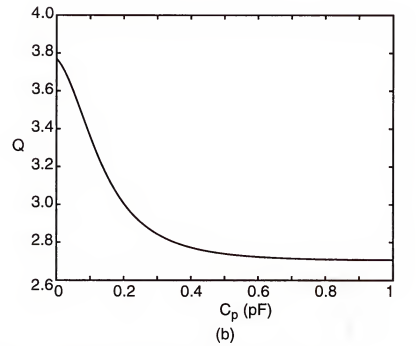


Figure 2-8 Q vs. R_{sub} (a) and Q vs. C_p plot (b).

These plots were generated using Matlab. For the Matlab simulation, L of 3 nH, and R_l of 10Ω are used. The operating frequency is assumed to be 2 GHz. For plot (a), C_p was assumed to be 250 fF and the R_{sub} was varied. This plot shows that R_{sub} should be either low or high to get high Q. This is understandable. When R_{sub} is low, the parasitic capacitor is close to ideal and it adds little loss. When R_{sub} is high, the branch with C_p and R_{sub} is close to open and the current on this branch is reduced. Therefore, once again, loss is reduced and higher Q can be obtained. In standard silicon processes, it is very difficult to get high substrate resistance. However, low substrate resistance is easier to achieve in standard silicon processes. A silicided polysilicon or a metal plane can be placed under the spiral of the inductor and connected to ground. This will shunt the substrate resistance and significantly lower the effective substrate resistance. However, the presence of a highly conductive plane under the spiral increases eddy current effect, which will reduce magnetic energy storage and will increase loss as explained in section 2.2.1. To reduce the eddy current while keeping the substrate resistance low, the polysilicon or metal ground plane should be patterned. This structure is called pattern ground shield (PGS). Figure 2-9 shows a patterned ground shield developed at the university of Florida. It has been shown that an addition of a PGS can increase Q by 25 to 30% compared to that of a conventional spiral inductor [Ton98, Yue98]. For plot (b), R_{sub} was assumed to be 400 Ω and C_p was varied. As expected, when C_p is low, Q is higher. This is because,

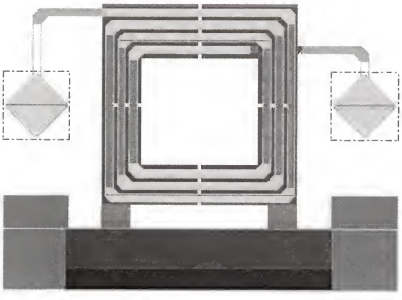


Figure 2-9 A layout of a pattern ground shield inductor test structure.

when C_p is low, less current is flowing on the C_p-R_{sub} branch and as a result lower power is dissipated in R_{sub}. In this simulation study, only one set of inductor model parameters was used. However, the conclusions apply to the most of the on-chip spiral inductors.

2.5 Biased n-well Inductor

In standard silicon technology, there are two common ways to improve Q. One way is making metal lines wider and the other is shunting multiple metal layers to lower the series resistance. The metal lines, however, cannot

be arbitrarily widened because of the area limitation and parasitic capacitance to substrate. Use of the first level metal in a shunting scheme also increases the parasitic capacitance. As shown in section 2.4.4, the presence of the parasitic capacitance decreases Q of an inductor. The parasitic capacitance in addition to lowering Q factor and self-resonance frequency of an inductor, reduces the resonance frequency of RF circuits using the inductors.

The effects due to the presence of an n-well with bias and no bias under spiral inductors are described in this section [Kim97]. Inductors with an underlying n-well are fabricated using a 0.8-μm CMOS process. The layout of the inductor is shown in Figure 2-10(a), and Figure 2-10(b) shows a cross section of the inductor. S-parameters are measured at different n-well bias conditions and the equivalent circuit model parameters are extracted and compared. The results show that, when the n-well-to-substrate junctions are reverse biased, parasitic capacitance associated with the inductors can be reduced approximately by a factor of 2 and the peak quality factor (Q) can be increased by ~10%. This reduction in the parasitic capacitance should enable widening of the inductor metal traces to increase the Q at low frequencies while keeping the parasitic capacitance and self resonance frequency constant [Kim97].

2.5.1 Inductor Design and Experiments

The inductor area is 145 x 145 μm^2. The metal width and space are 5.2 μm and 2 μm (i.e. 7.2-μm metal pitch). The inductor has 9.25 turns and its

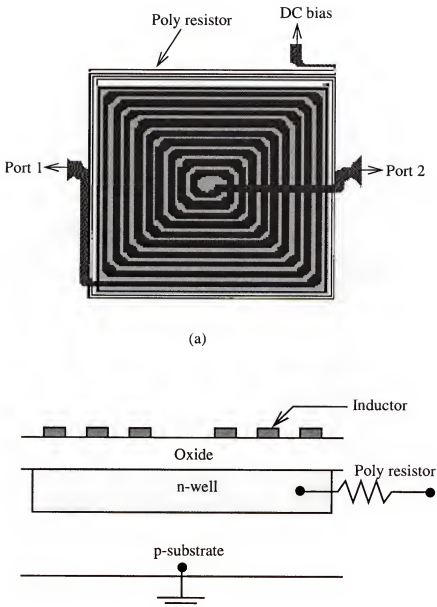


Figure 2-10 A Layout (a) and a cross section (b) of a biased n-well inductor.

inductance was estimated to be 6.2 nH using FastHenry [Kam93]. Three metal layers were shunted to reduce the series resistance. The sheet resistances are 0.05 Ω/❑ for the third level metal layer and 0.07 Ω/❑ for the first and second level metal layers. In addition to the metal trace of the inductor, there is a polysilicon spiral, which forms a resistor. This polysilicon resistor (~7kΩ) is connected between the n-well and dc bias for the n-well. The resistor isolates ac signals on the n-well node from the dc bias source or ac ground. S-parameters are measured over an n-well bias range between -5 V and 5 V. The equivalent circuit model in Figure 2-4(a) is used for the inductor parameter extraction. Series resistance (R_l), inductance (L) and parasitic capacitances associated with ports 1 and 2 were extracted from the low frequency (~700MHz) data. Each parasitic capacitor consists of an oxide capacitor between the metal line and n-well (C_{ox1}, C_{ox2}) and an n-well-to-p-substrate junction capacitor (C_{j1}, C_{j2}) in series (Figure 2-11). Because the total parasitic capacitances consist of the oxide and junction capacitances in series, the parasitic capacitances can be reduced by reducing the junction capacitances. The junction capacitance can be reduced by increasing the reverse bias between the n-well and p-substrate. The thickness of the oxide layer between the metal line and n-well is ~ 0.85 μm. Q-factors of inductors were estimated by using Q_{conv} defined by equation (2.24) which is valid at frequencies where the effects of parasitic capacitances are small.

2.5.2 Experimental Results and Discussion

The extracted inductance is 6 nH which agrees well with the designed value of 6.2 nH. The series resistance is estimated to be 15 Ω The inductance and series resistance were not changed with the changing n-well bias. Figure 2-12 shows plots of the parasitic capacitances, C_{p1} and C_{p2} versus n-well bias. C_{p1} is the total parasitic capacitance associated with port 1 (C_{ox1} and C_{j1} in series) and C_{p2} is the total parasitic capacitance associated with port 2 (C_{ox2} and C_{j2} in series) as shown in Figure 2-11. The capacitance between the n-well and metal lines does not change for the bias voltages between 0 and 5V because it is decided by the oxide thickness. When a negative bias voltage is applied to the n-well, this forward biases the junction, and the junction capacitance is increased by a large amount. Under this bias condition, the

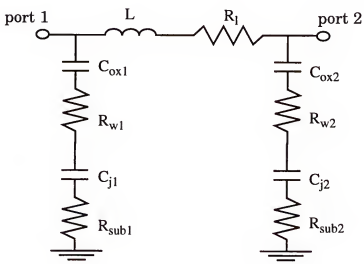


Figure 2-11 2-port equivalent circuit model for biased n-well inductor.

parasitic capacitances (C_{p1}, C_{p2}) are approximately equal to that of an inductor without the n-well. The measurements are consistent with the capacitance calculation based on the process data and the layout of the inductor. The calculated capacitance is ~350 fF. The junction capacitance decreases with the positive bias voltage on n-well which reverse biases the junction. Figure 2-12 shows that a 3-V reverse junction voltage reduces the parasitic capacitance by a factor little less than 2. In a separate experiment, it has been observed that when a dc bias voltage between 0 to 20 V is applied to the metal line of the inductor instead of the n-well, the parasitic capacitances change negligibly. The little changes in the parasitic capacitances are due to

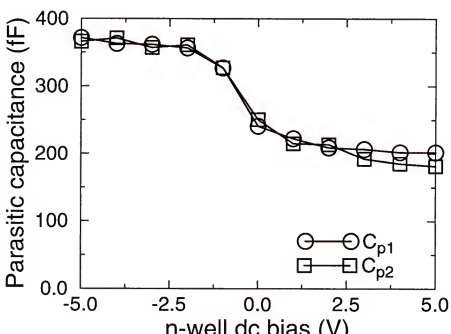


Figure 2-12 Parasitic capacitance with change of DC bias on n-well.

the fact that the steady state floating dc voltage of the n-well is 0 V regardless of the dc bias because of the leakage current associated with the junction. This means, all the dc bias voltage appears between the metal and n-well, and the junction capacitance changes negligibly with the bias on the inductor.

Figure 2-13 shows plots of conventional Q factor (Q_{conv}) versus frequency when a 3V, -1V, and no bias are applied to the n-well. Q_{conv} plots is almost the same among plots for the different bias conditions until the frequency is increased to ~1.3 GHz. It is observed that the peak Q factor for the

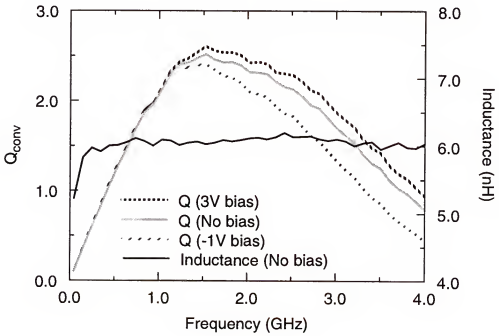


Figure 2-13 Measured Inductance(L) and Q_{conv} of biased n-well inductor with change of DC bias on n-well.

3-V n-well bias is about 10% higher than that with -1-V bias. The changes in the Q factors are mainly due to the changes in the parasitic capacitance. The small increase of the Q (~10%) compared to the large change in parasitic capacitance (~50%) indicate that other factors such as substrate resistivity and metal resistance also play a significant role in determining the Q.

As mentioned earlier, inductance and series resistance are not changed with the bias. Since the inductance remains the same, the self-resonance frequency varies because of the changing parasitic capacitance. The self-resonance frequency is 3.8 GHz at -5-V n-well bias. A 3-V n-well bias increases it to 5.8 GHz. A higher self-resonance frequency implies that the parasitic capacitance starts to reduce Q_{conv} at a higher frequency.

Because the inductors were fabricated on p on p^+ wafers, and the p-epitaxial layer is relatively thin, when the bias voltage is increased sufficiently, the depletion region reaches the p^+ region, and the increase of the depletion region or decrease of the capacitance slows. If the substrate has no p^+ region as well as having a lower doping as in some bipolar processes for RF applications [O95], the n-well bias can reduce the parasitic capacitance even more.

A report has shown that in a SiGe bipolar technology, having floating n-doped regions under inductors can reduce the peak Q [Bur96]. Measurements of inductors with and without an n-well fabricated in the CMOS technology used in this study, however showed that the peak Q is slightly higher when the well is included. It is speculated that this difference with the previ-

ous report [Bur96] is due to the fact that the resistivities of n-wells are similar or higher than in the heavier doped field isolation regions. Because of this, the eddy current effects are similar in both cases, while adding an n-well decreases the parasitic capacitances.

An ability to reduce the parasitic capacitance without affecting the inductance and series resistance is a useful feature for designing inductors for RF circuits. This feature can also be used to change the tune frequency of the RF circuits. This work demonstrated a method to decrease the parasitic capacitance by a factor little less than 2. This, in theory, can be used to widen the metal line by a factor of 2 or enable use of the 1st level metal in a shunting scheme to improve the low frequency Q by a factor of 2 while keeping the self-resonance frequency constant.

2.6 0.6-nH Inductors on SOI and SOS Substrates

2.6.1 Inductor Design

A 0.6 nH inductor was designed for the 13-GHz tuned amplifier which is described in Chapter 3. The inductor was fabricated on SOI and SOS substrates. The process has two metal layers. The layout of the inductor is shown in Figure 2-14. The inductor has 2.5 turns. The metal line width is 3 μm and the space is 2 μm (i.e. metal pitch is 5.4 μm). The area of the inductor is 52 x 52 μm^2. Once again, FastHenry was used for the inductor design and the estimated inductance is 0.6 nH. The first (M1) and second (M2) metal layers

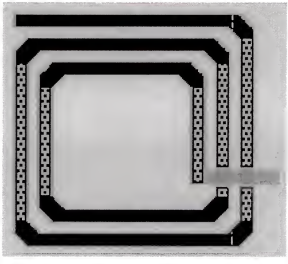


Figure 2-14 Layout of 0.6 nH inductor.

were shunted to reduce the series resistance. Sheet resistivities of the M1 and M2 are 0.05 and 0.08 Ω/□, respectively. Since SOS and SOI substrates are used for fabrications, the biased n-well was not used for these inductors.

2.6.2 Experimental Results and Discussion

The inductor model parameters were extracted from the S-parameter measurements. Figure 2-15 shows the inductance. The measured inductance is ~0.6 nH for both SOI and SOS inductors. Figure 2-16 shows Q_{BW} for the inductors. This plot shows similar Q estimation for both SOS and SOI induc-

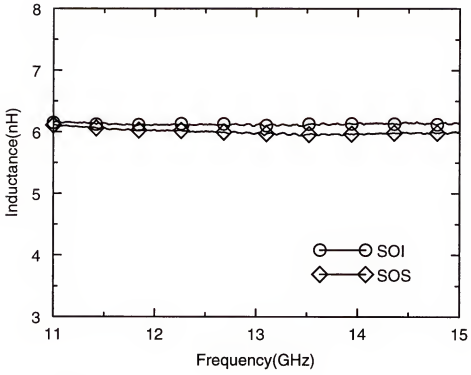


Figure 2-15 Inductance versus Frequency.

tors. The measured Q_{BW}'s are 8 and 6.5 at 12.5 GHz for SOS and SOI inductors, respectively. Q_{BW} of the SOS inductor is much higher than Q_{BW} of the SOI inductor at frequencies greater than 13.5 GHz.

The measurement results show that Q factors increase monotonically in the frequency range measured (up to 15 GHz), which means a further optimization (using wider metal lines) of the inductor to have peak Q's around their frequencies of use (12 ~ 13 GHz) is necessary. There is a good chance that higher Q will be achieved at the frequency of use through the optimization. Another implication is that the design of an inductor for ~20 GHz applications which are needed for the wireless clock distribution system should be

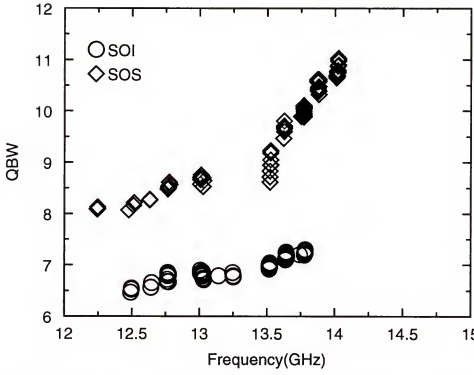


Figure 2-16 Q_{BW} versus Frequency plot for 0.6 nH inductor on SOS and SOI.

possible using this technology. Figure 2-17 shows the measured parasitic capacitances (C_p). The measured capacitances are ~15 fF and ~20 fF for the SOS and SOI inductors, respectively.

The SOS inductor shows higher Q and lower C_p than SOI due to its non-conductive substrate. The low parasitic capacitance and non-conducting substrate of SOS is beneficial for high frequency applications. The benefits of the non-conductive substrate will be even greater for larger inductors.

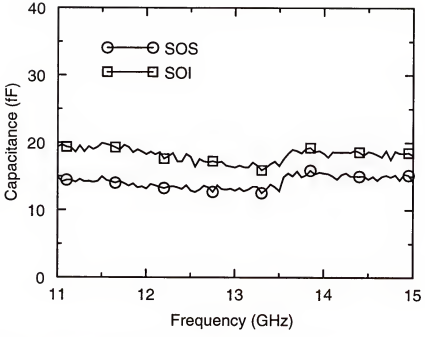


Figure 2-17 Parasitic capacitance (C_p) measurement.

2.7 Summary

A biased n-well inductor was implemented using a 0.8-μm CMOS process. A Biased n-well placed under a conventional spiral inductor reduces the coupling capacitance to the substrate and this increases Q. The measurements show that the coupling capacitance was reduced by about a half and Q-factor was increased by ~10%. Another benefit of the biased n-well inductor is the fact that the coupling capacitance can be changed by changing the bias to the n-well. This feature can be used to tune the resonance frequency of circuits without changing the inductor design.

A 0.6-nH inductor structure was implemented on SOS and SOI substrates. The measurements show that the SOS inductor has Q of 8 and the SOI inductor has Q of 6.5 at 12.5 GHz. The higher Q of the SOS inductor is due to lower parasitic capacitance and substrate loss. The measurements show that Q factors for the SOI and SOS increase monotonically between 11 and 15 GHz. This means that higher Q can be achieved through design optimization (using wider metal lines) to have higher peak Q at the frequency of interest (12~13 GHz for the amplifier discussed in Chapter 3). Another implication is that the implementation of inductors with reasonable Q for ~20 GHz applications which are needed for the wireless clock distribution system should be possible.

CHAPTER 3
TUNED AMPLIFIER

3.1 Introduction

Recent works have shown the potential of standard CMOS as a viable contender in the frequency range between 0.9 and 2 GHz for RF front-end receiver circuits [Kar96, Ho96, Sha97, Flo99]. As gate lengths decrease to 0.1 μm and below, this frequency range will increase, possibly opening up applications such as wireless LANs and DBS (Direct Broadcast Satellites) in the 10 to 20 GHz range. Though it will be difficult to surpass a GaAs MESFET LNA result [Shi94], CMOS technologies offer a potentially unique ability to integrate an entire receiver including base band and digital circuits onto a chip.

This chapter describes 13-GHz CMOS tuned amplifiers implemented using a partially scaled 0.1-μm CMOS process with partially-depleted SOS (Silicon on Sapphire) and SOI (Silicon on Insulator) NMOS transistors [Kim98, Ho98]. These are the first CMOS amplifiers to have tuned frequencies higher than 10 GHz. The wireless clock distribution system requires receiver circuits operating at ~ 20 GHz. This work shows that it is possible to design a CMOS tuned amplifier operating at frequencies greater than 10

GHz and 20-GHz tuned amplifiers can be implemented through design and process optimization.

3.2 Tuned Amplifier Design

3.2.1 Amplifier Architecture

A schematic of the amplifier is shown in Figure 3-1. All the transistors have floating bodies. Cascodes $M_{1,2}$ and $M_{3,4}$ provide all of the circuit gain.

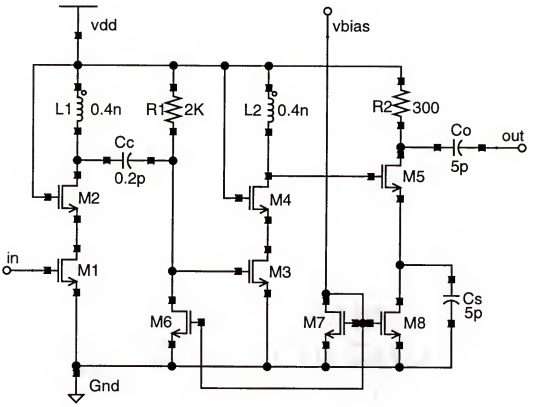


Figure 3-1 Schematic of 13 GHz Low Noise Amplifier.

Two gain stages are needed to have sufficient gain at 13 GHz. M_1 is biased through an input off-chip bias tee. Current mirrors $M_{6\text{-}8}$ bias the second cascode and the output buffer stage, M_5. The resonant frequency is set by two inductors, L_1 and L_2, and the total parasitic capacitances seen by these inductors. Since this amplifier uses two resonant gain stages, the total capacitances seen by the inductors should be carefully matched to avoid double resonant frequencies. At the resonance frequency (ω_0), the load impedance seen by each cascode stage is

$$Z_L\big|_{\omega=\omega_0} \cong \frac{(\omega_0 L)^2}{R_l} = Q\omega_0 L, \tag{3.1}$$

where $\omega_0 \cong 1/(\sqrt{LC_T})$, R_l is the series resistance of the inductor, C_T is the total capacitance seen by the inductor, and Q is the Q of the L-R_l series network ($Q=\omega L/R_l$). The voltage gain of the first stage can be approximated by

$$|A_{V1}| = \left|\frac{V_{D2}}{V_S}\right| \cong \frac{1}{\sqrt{1+(\omega_0 C_{GS1} R_S)^2}} \cdot (g_{m1} \cdot Z_L) \tag{3.2}$$

where V_{D2} is the voltage at the drain of M_2, C_{GS1} is the gate-to-source capacitance of M_1, and g_{m1} is the transconductance of M_1. The voltage gain of the second stage also can be approximately expressed the same way as in (3.2) except for the first term to account for the voltage division between the source impedance and input impedance of the cascode.

The coupling capacitor, C_C de-couples the drain-node of the first stage and the gate input of the second stage. R_1 and M_6 provide the DC bias for the

second stage. C_O is a de-coupling capacitor for DC isolation at the output. C_S grounds the source of M_5 at high frequencies. The capacitance at the source of M_5 can generate negative resistance at the gate of M_5. This negative resistance can cause stability problem. Therefore, C_s should be large enough so that the negative resistance is small. The impedance (Z_{in5}) looking into the gate of M_5 is

$$Z_{in5} \cong \frac{-g_{m5}}{\omega^2 \cdot C_{GS5} \cdot C_S} - j \cdot \left(\frac{1}{\omega \cdot C_S} + \frac{1}{\omega \cdot C_{GS5}} \right), \tag{3.3}$$

where g_{m5} and C_{GS5} are the transconductance and gate-to-source capacitance of M_5. Finally, a 10-pF on-chip bypass capacitor is integrated between V_{DD} and ground, minimizing the ground bounce problem due to the DC supply-line inductance. The Q factor of the bypass capacitor was kept moderate (~10) in order to avoid oscillation.

The transducer power gain of an amplifier is given in equation (3.4), assuming the amplifier is driven by a voltage source, V_S, with source impedance R_S, and loaded at the output by R_{Load} via transmission lines with characteristic impedances of R_S and R_{Load}, respectively [Gon84].

$$G_T = \frac{P_{Load}}{P_{AVS}} = |S_{21}|^2 = 4\left|\frac{V_{OUT}}{V_S}\right|^2 \frac{R_S}{R_{Load}} = 4|A_v|^2 \frac{R_S}{R_{Load}} \tag{3.4}$$

P_{Load} is the power delivered to the output load, P_{AVS} is the power available from the source, and V_{OUT} is the voltage at the output node of the amplifier.

Input and output matching networks are not integrated in the amplifiers, although a partial output matching is provided by the load resistor (R_2). The on-chip inductive degeneration for input matching is not used due to a concern for the negative effect of the series resistance of integrated spiral inductors to the gain and noise figure. Therefore, to obtain the maximum gain (G_{max}) and minimum noise figure (F_{min}), external matching networks are needed.

The primary sources of noise in this architecture include the channel thermal noise of M_1 and the channel thermal noise of M_2 [Ted94], both including the excess noise due to hot-electrons [Jin85], and noise from the second stage. Secondary sources of noise include the induced gate noise [Sha97, Zie86], substrate resistance, and thermal noise associated with the series resistance at the input (including gate resistance, metal 1 and metal 2 series resistance for connections, and contact resistance introduced by the measurement probes).

A microphotograph of the 13 GHz tuned amplifier is shown in Figure 3-2. The size of the circuit is 480 x 580 μm^2. The size of the output pad is 80 x 80 μm^2. A diamond-shaped pad was used on the input. It reduces the pad size by half and, as a result, it reduces the parasitic capacitance to the ground. The design is implemented in a partially-scaled double-metal, 0.1-μm CMOS process. A 0.35-μm design rule set is used for all dimensions except for the 0.1-μm gate length. The gate was patterned using X-ray lithography. The

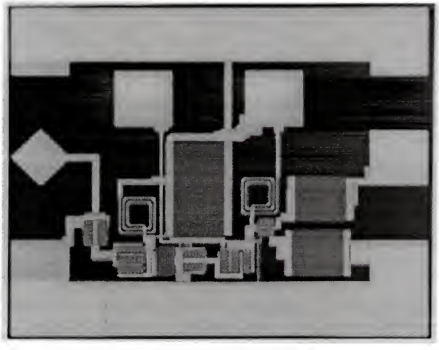


Figure 3-2 Microphotograph of 13 GHz tuned amplifier.

thickness of the gate oxide is 2.9-nm. The transistors have a measured peak f_T of approximately 100 GHz for both SOS and SOI transistors. Threshold voltages are 0.2 V and 0.4 V for the SOS and SOI transistors, respectively.

3.2.2 Inductor and Capacitor Design

The tuning inductors, $L_{1,2}$, are on-chip 0.6-nH spiral inductors. The design and characteristics of the inductors were described in section 2.6. Measured inductance is ~0.6 nH for both SOS and SOI inductors and Q-fac-

tors at 12.5 GHz are approximately 8 and 6.5 for the SOS and SOI inductors, respectively.

The capacitors were implemented using a high capacitance density MOS structure with the gate oxide layer as the dielectric [Hun98]. Figure 3-3 shows a cross section of the capacitor structure on an SOI and an SOS substrate. An issue for this structure is the parasitic bottom-plate to back-gate (p-substrate) capacitance on SOI substrates (Figure 3-3).

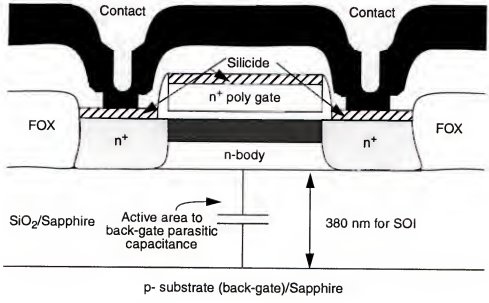


Figure 3-3 A cross-section of a MOS capacitor structure on SOI/SOS substrates.

3.3 Experimental Results

3.3.1 Measurement Set-up

The amplifiers have been characterized by measuring S-parameters, noise figure, F_{min} and IP3. All the parameters have been measured on-wafer using high frequency probes and a probe station. Noise figures have been measured using an HP8970B noise figure meter and an HP8971C noise figure test set. Noise figure test set increases the upper frequency limit of the noise figure meter from 1.6 GHz to 26.5 GHz. F_{min}'s have been measured using the measurement set-up shown in Figure 3-4. The measurement set-up consists of s microwave tuner, a noise source, and the noise figure meter with the noise test set. The F_{min} measurements have been done manually by changing the tuner position and searching for the minimum noise figure. The third order intercept point (IP3) and 1-dB compression points (P_{1dB}) have been measured using two microwave signal sources, a power combiner, and

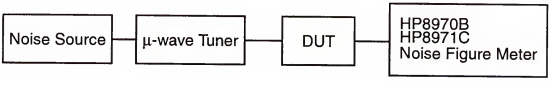


Figure 3-4 F_{min} measurement set-up.

an HP8563E spectrum analyzer. The spectrum analyzer can measure a frequency spectrum up to 26.5 GHz. The IP3 measurement set-up is shown in Figure 3-5. For IP3 and 1dB compression point measurements, outputs of the two signal sources should be combined with a power combiner and connected to the input of the amplifier. The spectrum analyzer is connected to the output of the amplifier and measures the power levels of the 1st and 3rd order harmonics. The input power (P_{in}) is computed using the power level from the power source (P_{avs}) and the input reflection coefficients of the amplifier. The P_{in} can be computed using the following equation.

$$P_{in} = P_{avs}(1 - |\Gamma_{in}|^2) \cong P_{avs}(1 - |S_{11}|^2) \tag{3.5}$$

IP3 and P_{1dB} can be obtained from the plot of the input power versus power levels of the 1st and 3rd order harmonics.

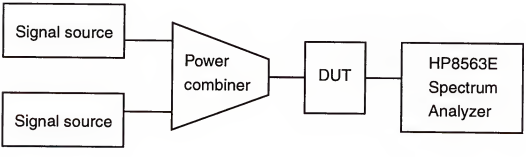


Figure 3-5 IP3 and 1-dB compression point measurement set-up.

3.3.2 Measurement Results

Figure 3-6 shows the transducer gain and 50-Ω noise figure data obtained using on-chip measurements for the 13-GHz amplifier with a supply voltage of 1.5 V. Peak gains of 15 dB at 13 GHz, and 5.3 dB at 12 GHz were measured for the SOS and SOI amplifiers, respectively. The difference in the resonant frequencies is due to the difference in the total capacitance to the substrate. The difference of gains and resonance frequencies for the SOS and SOI amplifiers will be discussed in section 3.4. The SOS amplifier exhibits

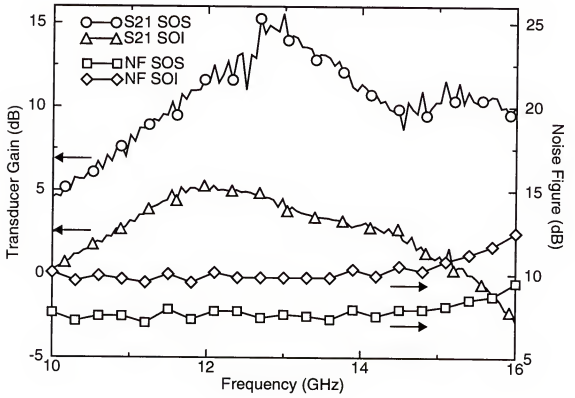


Figure 3-6 Transducer Gain and 50-Ω Noise Figure for SOS and SOI.

gains greater than 10 dB for frequencies up to 16 GHz, while the SOI amplifier has gains greater than 0 dB up to 15 GHz. The double peaks in the gain plots indicate a mismatch between the resonant frequencies of the first and second stages, caused by a difference in the total parasitic capacitances seen by the inductors L_1 and L_2. This mismatch decreases the amplifier's gain and Q. This measurement results imply that if the parasitic capacitances are estimated accurately and the amplifier design is optimized, a ~20 GHz tuned amplifier which is needed for the wireless clock distribution system could be possible.

The measured minimum noise figures (F_{min}'s) for the SOS and SOI amplifiers at ~13 GHz were 4.9 and 7.8 dB, as shown in Figure 3-7 along with the associated gains. The 50-Ω noise figures without any input matching were 7 dB and 9.1 dB for the SOS and SOI amplifiers at ~13 GHz, respectively. The high noise figures are partly due to the input not being closely matched to the Γ_{opt}. The higher noise figure for the 13-GHz SOI amplifier as compared to the 13-GHz SOS amplifier is primarily due to its lower power gain. There is also an additional noise source from the SOI back-gate which is coupled to the input of the amplifier primarily through the parasitic metal-to-back-gate capacitances associated with the input stage.

Input reflection coefficients (S_{11}) at the resonant frequencies for the 13-GHz amplifiers without the external microwave tuner are -2.5 and -3 dB for the SOS and SOI amplifiers, respectively. Output reflection coefficients

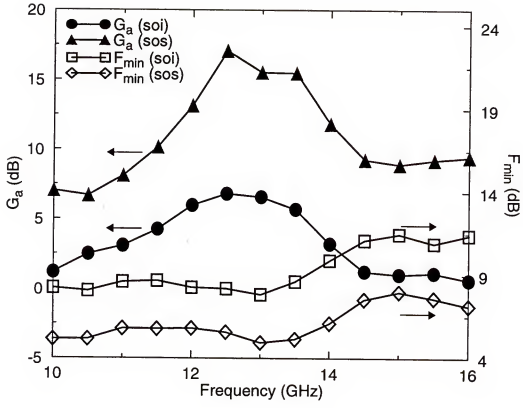


Figure 3-7 F_{min} for SOS and SOI

(S_{22}) at the resonant frequencies are -9.3 and -11 dB for the SOS and SOI amplifiers, respectively. Multiple-stage amplifiers typically have good isolation characteristics. Figure 3-8 shows the reverse isolation to be greater than 37 dB for both amplifiers. The measurements show that using SOS substrate over an SOI substrate does not improve the isolation. Figure 3-9 shows plots of the output power of the fundamental and third-order harmonic versus input power for the 13-GHz amplifiers. These plots indicate 1-dB compres-

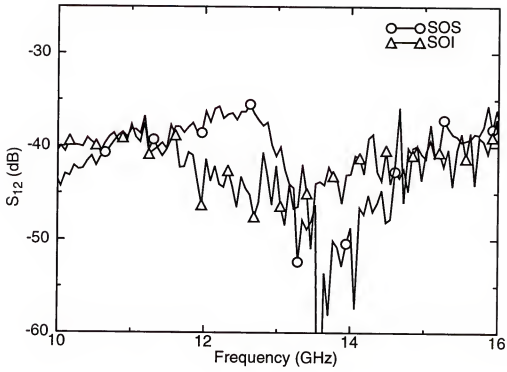


Figure 3-8 Reverse Isolation for SOS and SOI

sion points at the output of -24 and -22 dBm for the SOS and SOI amplifiers, respectively. Output-referred third-order intercept points (IP_3) are shown to be -16 and -18 dBm, respectively. The low compression points are primarily due to the voltage swing limitation at the output node of the last stage.

A summary of performance is shown in Table 3-1. These results provide an early look of the potential of both SOS and SOI technologies and of an anticipated fully scaled 0.1-μm bulk CMOS technology for high frequency RF circuit design.

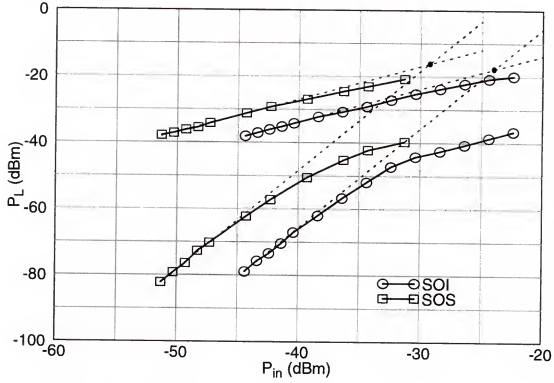


Figure 3-9 IP3 measurements for SOI and SOS amplifiers.

3.4 Discussion

The 13-GHz SOS amplifier has superior gain and noise characteristics as compared to the SOI amplifier. This gain difference is believed to be caused by parasitic capacitances from metal 1, metal 2, transistor, and capacitor active areas to the back-gate in the SOI amplifier (Figure 3-3). A relatively thin oxide layer between the metal 1 and back-gate (~0.7 μm) in this process exacerbated this problem. Though the back-gate is not physically

Table 3-1 13 GHz LNA performance summary

Substrate	SOI	SOS
Resonance frequency	12 GHz	13 GHz
Gain (S_{21})	5.3 dB	15 dB
Isolation (S_{12})	≤ -37 dB	≤ -37 dB
50-Ω Noise figure	9.1 dB	7 dB
Minimum F_{min}	7.8 dB (13 GHz)	4.9 dB (13 GHz)
1 dB compression (output)	-22 dBm	-24 dBm
IP3 (output)	-18 dBm	-16 dBm
Power consumption	45 mW	58 mW
Power supply	1.5 V	1.5 V

grounded, capacitive coupling between the back-gate and top-side metal ground bars effectively grounds the back-gate at high frequencies.

Figure 3-10 shows the SOISPICE [Fos97] simulation results for the power gain of the SOI amplifier with and without these parasitic capacitances to the back-gate. These simulations show that inclusion of these parasitic capacitances reduce the gain for the SOI amplifier by 8 dB. This reduction in gain leads to an increase in the noise figure. The power gain simulation results with the back-gate parasitic capacitances approximately match the measurements of the SOI amplifier, while the simulation results

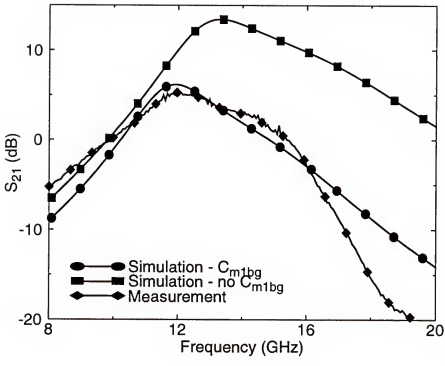


Figure 3-10 S_{21} measurement and simulation results with and without backgate parasitic capacitances for 13 GHz SOI amplifier.

without the backgate parasitic capacitances approximately match the measurements of the SOS amplifier. These suggest that if the layout is properly optimized and a better back-end process is used to reduce the back-gate parasitic capacitances, the performance of the 13-GHz SOI amplifier can be made to approach that of the SOS amplifier. This is consistent with the fact that the f_T's for the SOS and SOI transistors are approximately the same. Since the parasitics of the SOI devices in this process should be close to those in a fully scaled 0.1-μm bulk CMOS process, these discussions once again

suggest that 20-GHz amplifier circuits needed for the wireless clock distribution may be possible in a fully scaled bulk CMOS process.

As discussed in section 3.3.2, IP3 and P_{1dB} of both SOI and SOS amplifiers are low. As mentioned, the main reason for this is that the voltage swing at the output node is limited by the load resistance R_2 of the common source stage (Figure 3-1). Both output matching and the linearity of the 13-GHz amplifier can be improved by replacing the load resistor (R_2) of the output stage with an inductor and a capacitive transformer [O97].

3.5 Summary

This chapter described 13 GHz tuned amplifiers implemented on SOS and SOI substrates. This work showed the possibilities of the CMOS technology for RF applications above 10 GHz.

The amplifier has three stages. The first two stages are cascodes and they provide all the amplifier's gain. The last stage is a common source and is a buffer to drive the 50 Ω load. The SOI amplifier has 5.3-dB gain, 9.1-dB noise figure, -18-dBm IP3 at the output, and 7.8-dB F_{min}. The SOS amplifier has 15-dB gain, 7-dB noise figure, -16-dBm IP3 at the output, and 4.9-dB F_{min}. Power consumption is 45 mW and 58 mW for the SOI and SOS amplifiers, respectively, on a 1.5 V power supply. The measurement results show that the SOS amplifier has gains greater than 10 dB up to 16 GHz. This result implies that ~20-GHz tuned amplifier which is needed for the wireless

clock distribution system may be possible to fabricate through proper accounting of the parasitics and design optimization.

This chapter also suggested a possible reason for the lower gain and resonance frequency of the SOI amplifier and suggested an architectural improvement using a capacitive transformer to increase IP3.

CHAPTER 4
ANTENNA TEST STRUCTURE AND MEASUREMENT SET-UP

4.1 Introduction

The performance of antennas are estimated by measuring antenna parameters such as radiation resistance, directivity, antenna efficiency, and input impedance. These parameters are related to each other. To understand the performance of antennas, it is necessary to understand the relationships between the parameters and their origins. In this chapter, fundamental antenna parameters are described. Understanding of these parameters will help interpreting the measured antenna data. To design an antenna, the fundamental field properties of the basic antenna type need to be understood. The electromagnetic field analysis of short dipole and loop antennas are presented in this chapter. Although the presence of substrates near antennas for on-chip antennas will alter the field characteristics, the field analysis of basic antennas provides insights in designing the on-chip antennas. Antenna test structures which have been fabricated for experiments are presented and discussed. An antenna measurement set-up using baluns and signal-signal probes is also described.

4.2 Antenna Fundamentals

4.2.1 Antenna Parameters

This section summarizes key antenna parameters. More detailed discussions of these parameters can be found elsewhere [Kra88, Bal82].

Radiation Resistance

Radiation resistance (R_r) relates the radiation power of an antenna and input current (I). To compute the radiation resistance, total power radiated should be computed. This power is then equated to I^2R_r. The radiation resistance can be obtained from dividing the total radiated power by a square of the current. The total radiated power can be computed by integrating the average Poynting vector on a large sphere surrounding the antenna.

Input Impedance

Input impedance (Z_A) is defined as the impedance presented by an antenna at its terminals or the ratio of the voltage to current at the terminals with no load attached.

$$Z_A=R_A+jX_A \tag{4.1}$$

For an on-chip antenna, the input impedance is due to radiation impedance, loss resistance and capacitance of the metal structures of the antenna, and substrate impedance. The loss resistance comes from the conduction loss of the antenna structure. The capacitance of the metal structure is due to the capacitance between the metal and substrate. The substrate impedance

includes substrate resistance and capacitance associated with the semiconducting substrate.

Antenna Efficiency

The total antenna efficiency is used to take into account losses at the input terminals and within an antenna structure. The total efficiency (e_t) can be expressed as

$$e_t = e_r e_c e_d \tag{4.2}$$

where e_r is the reflection efficiency which comes from the mismatch between antenna input impedance and characteristic impedance of a transmission line. e_r can be expressed as $e_r = 1 - |\Gamma_{in}|^2$, where Γ_{in} is the reflection coefficient. Γ_{in} is

$$\Gamma_{in} = \frac{Z_{in} - Z_o}{Z_{in} + Z_o}. \tag{4.3}$$

Z_{in} is the input impedance of the antenna and Z_o is the characteristic impedance of the transmission line. e_c is the conduction efficiency which accounts for conduction loss and e_d is the dielectric efficiency which accounts for the dielectric loss. Usually e_c and e_d are very difficult to compute, but they can be determined experimentally. Even by measurement they can not be separated and they are usually lumped together to form the conductor-dielectric efficiency e_{cd}. The conductor-dielectric efficiency (equation (4.4)) is defined as the ratio between the power radiated and the power delivered to the $R_r + R_{loss}$ where R_{loss} is used to represent the conductor-dielectric losses.

$$e_{cd} = \frac{R_r}{R_r + R_{loss}}. \tag{4.4}$$

Directivity

The directivity of an antenna is defined as the ratio of the radiation intensity in a given direction from the antenna to the radiation intensity averaged over all directions. The average radiation intensity is equal to the total power radiated by the antenna divided by 4π. If the direction is not specified, the direction of maximum radiation intensity is implied. The directivity can be expressed as

$$D(\theta, \phi) = \frac{U(\theta, \phi)}{U_0} = \frac{4\pi U(\theta, \phi)}{P_{rad}}, \tag{4.5}$$

where D is the directivity, U is the radiation intensity, U_0 is the radiation intensity of an isotropic source, and P_{rad} is the total radiated power.

Gain

The gain of an antenna is defined as the ratio of the radiation intensity, in a given direction, to the radiation intensity that would be obtained if the power delivered to the antenna were radiated isotropically. The radiation intensity corresponding to the isotropically radiated power is equal to the power delivered to the antenna divide by 4π.

$$G(\theta, \phi) = 4\pi \frac{RadiationIntensity}{TotalInputPower} = \frac{4\pi U(\theta, \phi)}{P_{in}}. \tag{4.6}$$

In most cases, we deal with relative gains which are defined as the ratio between the power gain in a given direction and power gain of a reference antenna in a reference direction. The reference antenna can be a dipole, a horn, or any other antennas whose gains can be calculated or are known. In most cases, however, the reference antenna is a lossless isotropic source. When the direction is not specified, the power gain is usually taken in the direction of maximum radiation. According to the IEEE standards, gain does not include losses arising from impedance mismatches and polarization mismatches. The total radiated power is related to the total input power by $P_{rad} = e_{cd}P_{in}$. From equations (4.5) and (4.6), gain can be related to the directivity by

$$G(\theta, \phi) = e_{cd}D(\theta, \phi). \tag{4.7}$$

Effective Aperture

The effective aperture describes the power capturing characteristics of an antenna. The effective aperture is defined as the ratio of power delivered to the load to the power flux density of a plain wave incident on the antenna. If the direction is not specified, then, once again, the direction of maximum radiation intensity is implied. An antenna and its equivalent circuit are shown in Figure 4-1. The effective aperture (A_e) is

$$A_e = \frac{P_T}{W_i} = \frac{|I_T|^2 R_T}{2W_i}, \tag{4.8}$$

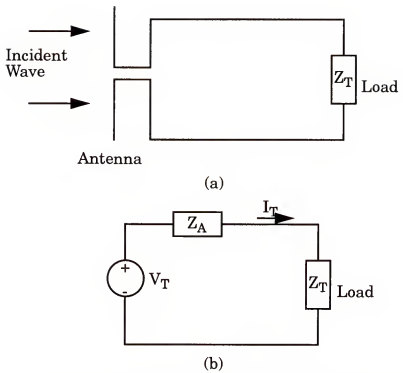


Figure 4-1 Antenna in a receiving mode (a) and its equivalent circuit (b).

where P_T is the power delivered to the load, R_T is the load resistance, and W_i is power density of an incident wave. The effective aperture is the area which gives the power delivered to the load when multiplied by the incident power density. If we assume the load impedance is $Z_T=R_T+jX_T$, then equation (4.8) becomes

$$A_e = \frac{|V_T|^2}{2W_i}\left[\frac{R_T}{(R_A+R_T)^2+(X_A+X_T)^2}\right] \tag{4.9}$$

Under the maximum power transfer conditions (conjugate matching), the effective aperture becomes the maximum given by

$$A_{em} = \frac{|V_T|^2}{8W_i}\left[\frac{1}{R_A}\right] \quad . \tag{4.10}$$

In general, the maximum effective aperture of an antenna is related to its maximum directivity by

$$A_{em} = \frac{\lambda^2}{4\pi}D_0 . \tag{4.11}$$

Equation (4.11) assumes that there are no conductor-dielectric losses, the antenna is matched to the load, and the polarization of the incident wave is matched to that of the antenna. If there are conductor-dielectric losses, equation (4.11) should be modified to

$$A_{em} = e_{cd}\left(\frac{\lambda^2}{4\pi}\right)D_0 \quad . \tag{4.12}$$

Friis' Transmission Formula

The Friis' transmission formula relates the power received to the power transmitted between two antennas separated by a distance $R>2L^2/\lambda$, where L is the largest dimension of either antenna. If the input power at the terminals of the transmitting antenna is P_t, then the isotropic power density W_0 at distance R from the antenna is

$$W_0 = \frac{e_{cdt}P_t}{4\pi R^2} \tag{4.13}$$

where e_{cdt} is radiation efficiency of the transmitting antenna. For an anisotropic transmitting antenna, the power density of equation (4.13) in the direction θ_t, ϕ_t can be written as

$$W_t = \frac{P_t G_t(\theta_t, \phi_t)}{4\pi R^2} = e_{cdt}\frac{P_t D_t(\theta_t, \phi_t)}{4\pi R^2} \tag{4.14}$$

where G_t is the gain and D_t is the directivity of the transmitting antenna. Since the effective aperture A_r of an antenna is related to its efficiency e_{cdr} and directivity D_r by

$$A_r = e_{cdr} D_r(\theta_r, \phi_r)\left(\frac{\lambda^2}{4\pi}\right). \tag{4.15}$$

The amount of power P_r collected by the receiving antenna can be written as

$$P_r = e_{cdr} D_r(\theta_r, \phi_r)\left(\frac{\lambda^2}{4\pi}\right) W_t = e_{cdr} e_{cdt}\frac{\lambda^2 P_t D_t(\theta_t, \phi_t) D_r(\theta_r, \phi_r)}{(4\pi R)^2}. \tag{4.16}$$

This formula does not include the reflection efficiency. If the reflection efficiency of the receiving and transmitting antenna are included, the ratio between the received power and input power can be represented by

$$\frac{P_r}{R_t} = |S_{21}|^2 = e_{cdr} e_{cdt}(1 - |\Gamma_r|^2)(1 - |\Gamma_t|^2) D_r(\theta_r, \phi_r) D_t(\theta_t, \phi_t)\left(\frac{\lambda}{4\pi R}\right)^2, \tag{4.17}$$

where Γ_t and Γ_r are the reflection coefficients of transmitting and receiving antennas, respectively. This equation is known as Friis' transmission formula.

4.2.2 Short Dipole Antenna

The characteristics of a linear dipole antenna is well known. This section summarizes the characteristics of a short dipole antenna. Detailed analyses and derivations of the equations can be found elsewhere [Kra88, Bal82].

A short dipole is electrically small (l << λ) dipole and thin (d << l). l is the length and d is the thickness of the antenna, and λ is the wavelength. The short dipole antenna analysis is important because any linear dipole antenna can be considered as a large number of short dipole antennas connected in series.

The current in a short dipole antenna is assumed to be constant. If we assume a dipole antenna with a length l is at the origin along the z-axis, the vector potential $\overline{A}$ can be computed as follows

$$\overline{A}(R) = \frac{\mu}{4\pi}\int \frac{\bar{I}}{R} e^{-jkR} dl = \frac{\mu l I_0}{4\pi r} e^{-jkr}\hat{z}. \tag{4.18}$$

Since $\bar{I}=I_0\,\hat{z}$ and $R=\sqrt{(x-x')^2+(y-y')^2+(z-z')^2} \cong \sqrt{x^2+y^2+z^2} = r$ (l << λ), where $\bar{r}=(x,y,z)$ represents field point and $\bar{r}' = (x', y', z')$ represents source point. Once the vector potential is computed, then, H-field and E-field can be obtained using

$$\overline{H} = \frac{1}{\mu}\nabla\times\overline{A} \tag{4.19}$$

$$\overline{E} = \frac{1}{j\omega\varepsilon}\nabla\times\overline{H}. \tag{4.20}$$

The computed H and E fields using the above equations are

$$H_r = H_\theta = 0 \tag{4.21}$$

$$H_\phi = j\left(\frac{kI_0 l \sin\theta}{4\pi r}\right)\left[1 + \frac{1}{jkr}\right]e^{-jkr} \tag{4.22}$$

$$E_\phi = 0 \tag{4.23}$$

$$E_r = \eta\left(\frac{I_0 l \cos\theta}{2\pi r^2}\right)\left[1 + \frac{1}{jkr}\right]e^{-jkr} \tag{4.24}$$

$$E_\theta = j\eta\left(\frac{kI_0 l \sin\theta}{4\pi r}\right)\left[1 + \frac{1}{jkr} - \frac{1}{(kr)^2}\right]e^{-jkr} \tag{4.25}$$

The intrinsic impedance of air, $\eta = \sqrt{\frac{\mu_0}{\varepsilon_0}}$, is $120\pi\Omega$

The outgoing power density from the antenna can be written as

$$P = \frac{1}{2}\iint (E \times H^*) \cdot ds = \eta\left(\frac{\pi}{3}\right)\left|\frac{I_0 l}{\lambda}\right|^2\left[1 - j\frac{1}{(kr)^3}\right]. \tag{4.26}$$

The time average radiated power is

$$P_{rad} = Real(P) = \eta\left(\frac{\pi}{3}\right)\left(\frac{I_0 l}{\lambda}\right)^2, \tag{4.27}$$

and the radiation resistance can be computed from (4.27) as

$$R_r = \frac{P_{rad}}{I_0^2} = \eta\left(\frac{\pi}{3}\right)\left(\frac{l}{\lambda}\right)^2 = 80\pi^2\left(\frac{l}{\lambda}\right)^2. \tag{4.28}$$

At a distance kr=1(or r=$\lambda/2\pi$), which is referred to as the radian distance, the two term inside the bracket of (4.26) is the same. In the region r < $\lambda/2\pi$, the imaginary part of the power density, or reactive power density dominates. This region is referred to as the near field region. The region r > $\lambda/2\pi$ is

referred to as the intermediate region while r >> $\lambda/2\pi$ is referred to as the far field region. In the intermediate or far field region, radiated power density dominates over reactive power density. The reactive energy represents the energy storage oscillating back and forth from electric to magnetic energy storage, which does not propagate.

Equation (4.28) shows that the radiation resistance of short dipole antennas are very small (8Ω for $\lambda/10$ antenna). Small radiation resistance usually means low efficiency. Because of the low efficiency, short antennas ($l < \lambda/10$) are not widely used and moderate length dipole antennas ($l > \lambda/3$) are preferable.

4.2.3 Loop Antenna

Small loop antennas have similar characteristics as a small dipole antenna. Its characteristics are also well understood [Bal82, Ove96].

The geometry for analyzing a circular loop antenna is shown in Figure 4-2. When the antenna current distribution is known, once again, the vector potential can be computed using

$$\bar{A}(x, y, z) = \frac{\mu_0}{4\pi}\int_C \tilde{I}_e(x', y', z')\frac{e^{ikR}}{R}dl' \tag{4.29}$$

If the current is assumed to be constant ($\tilde{I}_e = I_0\hat{\phi}$) and runs along the wire loop in the ϕ direction, Eq. (4.29) simplifies to a single vector potential component.

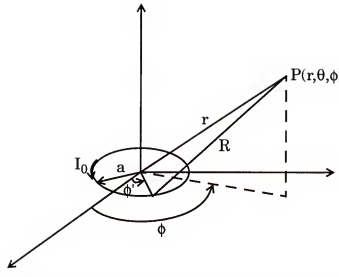


Figure 4-2 Geometry for a circular loop antenna analysis.

$$A_\phi(r,\theta,\phi) = \frac{aI_0\mu_0}{4\pi}\int_0^{2\pi}\cos(\phi-\phi')\frac{e^{ikR}}{R}d\phi' \tag{4.30}$$

with

$$R = \sqrt{r^2+a^2-2ar\sin\theta\cos(\phi-\phi')} \tag{4.31}$$

Since the current on the loop is constant and the antenna structure is symmetric, the field radiated by the loop antenna is not a function of angle ϕ. Thus, ϕ can be set to zero. To compute the vector potential, Eq. (4.30) must be integrated. This equation can not be integrated without any approximations. For small loops, $\frac{e^{-ikR}}{R}$ can be expanded using a Maclaurin series [Kre83]. If we take only the first two terms, the vector potential reduces to

$$A_\phi(r,\theta,\phi) \cong \frac{aI_0\mu}{4\pi}\int_0^{2\pi}\cos\phi'\left[\frac{1}{r}+a\left(\frac{jk}{r}+\frac{1}{r^2}\right)\sin\theta\cos\phi'\right]e^{-ikr}d\phi' \tag{4.32}$$

$$A_\phi(r, \theta, \phi) \cong \frac{a^2 I_0 \mu}{4\pi}\left(\frac{jk}{r} + \frac{1}{r^2}\right)\sin\theta e^{-ikr} \tag{4.33}$$

The magnetic field can be obtained using Eq. (4.19).

$$H_r = \frac{jka^2 I_0 \cos\theta}{2r^2}\left[1 + \frac{1}{jkr}\right]e^{-ikr} \tag{4.34}$$

$$H_\theta = -\frac{(ka)^2 I_0 \sin\theta}{4r}\left[1 + \frac{1}{jkr} - \frac{1}{(kr)^2}\right]e^{-ikr} \tag{4.35}$$

$$H_\phi = 0 \tag{4.36}$$

The electric field can be computed from the magnetic field using (4.20).

$$E_r = E_\theta = 0 \tag{4.37}$$

$$E_\phi = \eta\frac{(ka)^2 I_0 \sin\theta}{4r}\left[1 + \frac{1}{jkr}\right]e^{-ikr} \tag{4.38}$$

The field radiated by a small loop, as given by the above equations, are valid everywhere except at the origin.

The total complex power from a loop antenna can be written as

$$P = \frac{1}{2}\iint(E \times H^*) \cdot ds = \eta\left(\frac{\pi}{12}\right)(ka)^4 |I_0|^2\left[1 + j\frac{1}{(kr)^3}\right] \tag{4.39}$$

The total radiated power is the real part of Eq. (4.39).

$$P_{rad} = \eta\left(\frac{\pi}{12}\right)(ka)^4 |I_0|^2 \tag{4.40}$$

From $P_{rad} = |I_0|^2 R_r/2$, R_r is

$$R_r = \eta\left(\frac{\pi}{6}\right)(ka)^4 \tag{4.41}$$

In general, the radiation resistance of a single-turn small loop antenna is much smaller than the loss resistance. Thus, the corresponding radiation efficiencies (Eq. (4.4)) are very low and depend strongly on the loss resistance. The radiation efficiency of loop antenna can be improved by using multi-turn and a ferrite core. These antennas are typically used for receiving antennas due to their compactness and a good signal to noise ratio.

4.2.4 Balanced Versus Unbalanced Systems

For a two conductor circuit, an unbalanced system is defined as one in which the two conductors are above and below the ground potential by a different amount [Wee68] and consequently, the current in the two conductors may be different. In contrast, a balanced system is the one in which the two conductors are respectively above and below the ground potential by the same amount.

In the disciplines of antenna and transmission line, two halves of a symmetric transmission line or an antenna system are said to be balanced if they carry the same current, and unbalanced if their currents are unequal. This extension of meaning is helpful in practice because the detrimental effects of unbalanced systems (i. e., extra parallel wire transmission line loss to ground or in radiation, and a disturbed antenna pattern) are directly due to the current imbalance. Ordinarily, an imbalance of potentials with respect to ground causes the unbalanced current flow.

Typically, the feeding line to an antenna is a coaxial cable or parallel metal lines which is single-ended or unbalanced. To reduce the balanced-to-unbalanced mismatch loss, baluns are used to connect the coaxial cable or parallel metal lines to a balanced antenna such as a dipole antenna [Kaw91]. "Balun" stands for balanced-to-unbalanced transformer. For low frequency applications, transformer or choke type baluns are used, and, for high frequency applications, hybrid coupler type baluns are used [Sil84, Poz90]. In this work, 180^{o} hybrid couplers are used in the antenna measurement system to reduce the balanced-to-unbalanced mismatch loss.

4.3 Antenna Test Structures

To evaluate the performances of on-chip antennas, antenna test structures were fabricated using IBM and UF processes. The IBM process is a standard CMOS process. Antenna test structures were fabricated along with other test circuits. Because of the limitation in chip size, only two pairs of antennas were included. These test structures provide a realistic situation for studying on-chip antenna performance. Since the test structures include obstacles (test circuits) in between the antenna pairs, the measured performance includes interference effects from the obstacles. At the same time, the performance of antennas without any obstacles in between the receiving and transmitting antennas are necessary. In order to fabricate a wider range of test antennas in a large chip, the UF antenna fabrication process was developed. The antenna test structures on silicon substrates are fabricated at the

microelectronics lab in the University of Florida. The antenna fabrication process is described in Appendix A. The maximum wafer size which can be used in the process is 3 inch. The maximum size of the test structure is limited by the maximum wafer size and it is about 5x4 cm^2. This process is cheap and gives freedom to design various designs of antenna test structures with and without obstacles. Three sets of test structures were designed and fabricated using this process.

The antennas fabricated on substrates are called printed antennas [Jam87, Poz83, Rag90]. Widely used printed antennas include microstrip, dipole, and loop antennas [Car81, Kat83, Hej94]. Microstrip antennas are used for satellite communications and printed dipole antennas are studied for use in personal network hand set [Yu92]. The structure of a typical microstrip antenna is shown in Figure 4-3. The characteristics of microstrip antennas are well understood [Poz82, Car81, Lin95]. The microstrip antenna is unbalanced with respect to ground. Therefore, baluns are not necessary and the feeding structure is simple. The resonance frequency can be changed and the surface wave from the antenna can be suppressed by changing the shape of the patch or the thickness and dielectric constant of the substrate [Jac93, Pap95, Kok97]. The surface wave is considered as a loss in general communication antennas. Microstrip antennas are much bigger than dipole or loop antennas and requires a good ground plane and a lossless dielectric substrate as shown in Figure 4-3. For the wireless interconnection applications, these are serious drawbacks. Since the chip area is limited and expen-

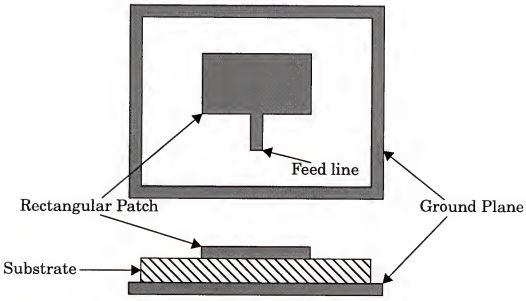


Figure 4-3 Rectangular microstrip antenna structure.

sive, a major determining factor for choosing an antenna is its size. On the other hand, a good ground plane is not usually available in silicon chips and silicon substrate is lossy. Because of these drawbacks, microstrip antennas are not included in the antenna test structure.

Printed dipole antennas on dielectric substrates have received a great deal of attention [Ran81, Uzu79, Mac95]. This is mainly due to its small size compared to microstrip antennas. One drawback of this antenna is that, since it needs a balanced input signal, a complicated feed structure including baluns is required. However, if a differential amplifier is used, then baluns are not necessary and the feed structure becomes simple balanced wires. As

for the microstrip antenna, the thickness and permittivity of the substrate affect the input impedance and radiation characteristics of the antenna [Kat83, Ale83]. The characteristics of dipole antennas can be also changed by using shaped arms. Meander, zigzag, and Archimedes spiral antennas have been studied [Nak84, Nak88, Ton94, Hir95]. The configurations of dipole antenna structures are shown in Figure 4-4. Among these antenna structures, the spiral antennas are not used in this work due to its relatively large size. Changes of feature sizes and angles of zigzag and meander antennas

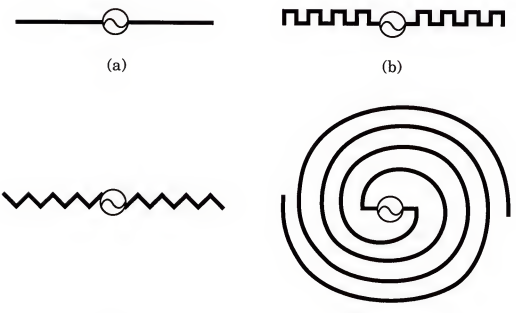


Figure 4-4 Configurations of printed dipole antennas: (a) Linear, (b) Meander, (c) Zigzag, (d) Spiral.

modify the antenna characteristics, and the antenna geometry must be optimized for better matching and antenna gain.

Printed loop antennas have also been studied [Hej94, Kha96]. Printed loop antennas can be compact and have an isotropic radiation pattern on the substrate plane. The isotropic radiation pattern is desirable for transmitting antennas for the wireless interconnection system because it alleviates the placement restrictions of receiving antennas. Loop antennas, especially single turn loop antennas, are known to have low power efficiencies [Bal82]. However, it has been shown that loops on dielectric substrates can have reasonable gains [Hej94].

From the above literature review, linear, meander, zigzag dipole, and loop antennas were chosen for experimental studies. The test structures were fabricated using the IBM and UF processes on bulk, SOI, and SOS substrates. The designs and substrate types of IBM testchips and the three UF chips will be presented in this section, and the measurement results will be presented and discussed in sections 5.3 ~ 5.6.

4.3.1 IBM Testchip

The antenna testchip was fabricated using an IBM 0.1-μm CMOS process. Linear dipole antennas were fabricated on 5 Ω-cm bulk, SOI (on 10 Ω-cm substrate), and SOS substrates (Figure 4-5) along with test circuits. The IBM process has two metal layers with no passivation. Two pairs of antenna test structures were fabricated using a ~0.6 μm thick metal layer (a pair of 4-mm

long and 4–μm wide antennas and a pair of 2-mm long and 1-μm wide antennas). The distances between receiving and transmitting antennas for the 4-mm antenna pair and 2-mm antenna pair are 2 mm and 4 mm, respectively. The antenna size and distance between receiving and transmitting antennas were limited by the chip size. The antenna sizes correspond to 0.2λ and 0.4λ at 15 GHz in oxide layer, and 0.1λ and 0.2λ in air.

Figure 4-6 shows a cross-section of on-chip antenna structures. Dielectric constants of bulk, SOI, and SOS substrates are ~ 12. Dielectric constant of oxide is 3.9. The thickness of the substrate is ~0.5 mm for all substrates (SOS, SOI, bulk). The oxide thickness is ~1.5μm.

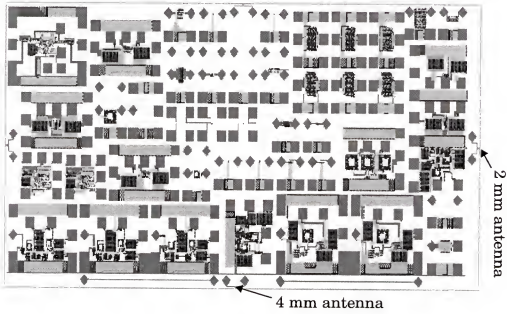


Figure 4-5 The chip layout which contains 2 mm and 4 mm antennas fabricated using IBM 0.1-μm CMOS process.

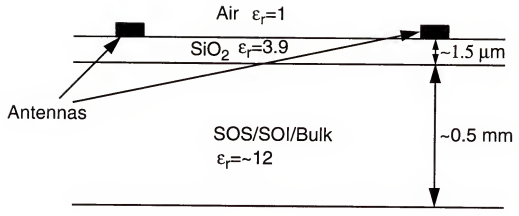


Figure 4-6 A cross-section of on-chip antennas.

4.3.2 1st UF Testchip

The UF process has one metal layer with no passivation. The 1st UF antenna testchip shown in Figure 4-7 was fabricated using the process [Kim98, Kim99]. The fabrication procedure is described in Appendix A. Blank 3-inch silicon wafers were used for the fabrication. The wafers are put into an oxidation furnace to grow an oxide layer about 1.5-μm thick. After the oxidation, 1.5-μm thick aluminum layer is deposited using an electron beam evaporator. Antennas are patterned using a mask aligner and a wet aluminum etch.

The testchip includes structures for characterizing the radiation patterns and transmission gain dependence on distance for linear, meander, and

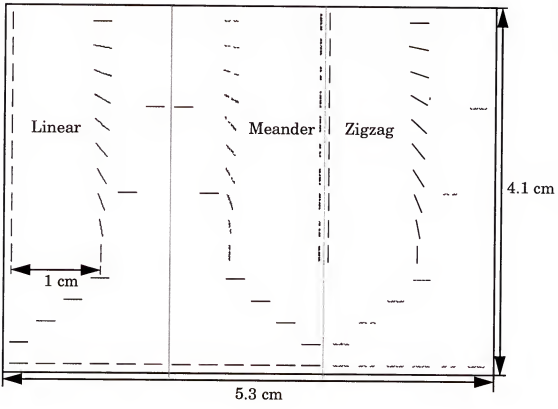


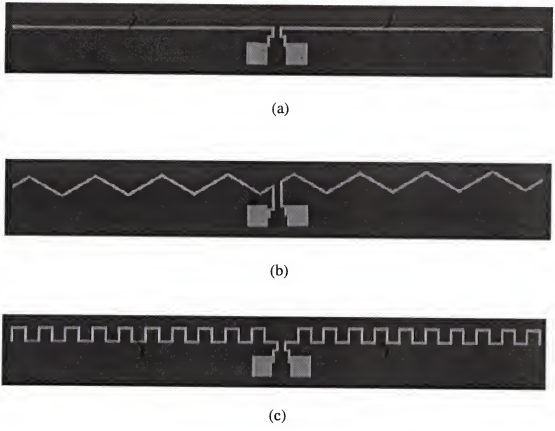
Figure 4-7 The layout of antenna the 1st UF testchip for linear, meander and zigzag dipole antennas.

zigzag dipole antennas (Figure 4-7). The transmission gain will be defined in section 5.3.1. For on-chip antennas, once they are placed, it is not possible to rotate or move the antennas. Therefore, in order to measure radiation patterns, antenna pairs whose axes are oriented with specific angles were designed. Since the radiation pattern of a dipole antenna is symmetric, the angle was varied from 0 to 90 degrees to generate a whole radiation pattern (0 to 360 degree). 10 pairs of antennas with a 10-degree increment have been implemented in this testchip. The distance between receiving and transmit-

ting antenna pairs for the radiation pattern measurements is 1 cm. The other structures for measuring the transmission gain dependence on distance has separations of 2.5, 5, 7.5, 10, 20, and 30 mm.

The antenna designs are similar to those in reference [Nak84]. The size of the testchip is 4.1 cm x 5.3 cm. This is around two times the projected size of ICs in the year 2010. The chip was fabricated on 5-Ω-cm 3-inch silicon wafers. The thickness of the wafer is 500 μm. Figure 4-8(a) is a microphotograph of a linear dipole antenna. The antenna length is 2 mm and the width is 10 μm. Figure 4-8(b) shows a zigzag dipole antenna. The axial length is 2 mm and the length of the arm element is 75 μm. The angle between adjacent arm elements is 120°. Figure 4-8(c) shows a meander dipole antenna. The axial length is 2 mm and arm element length is 60 μm.

Characteristics of the dipole antennas, such as gain, input impedance, and radiation pattern, can be changed by changing the axial length of the antennas [Bha91, Ran81]. Zigzag and meander dipole antennas give us more freedom to design than linear dipole because antenna characteristics, especially the input impedances, can be controlled by changing the length of arm elements as well as bend angle between the arm elements. This dependence of antenna characteristics on the arm element designs and axial lengths of dipole antennas are included in the 2nd UF testchip.



(a)

(b)

(c)

Figure 4-8 Microphotograph of linear dipole (a), zigzag dipole (b), and meander dipole (c) antennas.

4.3.3 2nd UF Testchip

The layout of the 2nd UF antenna testchip is shown in Figure 4-9. The size of the testchip is 4.3 x 4.7 cm^2. This testchip was fabricated on 10 Ω-cm and 20 Ω-cm silicon substrates with an oxide layer thickness of 1, 3, 9 μm. An SOS wafer is also used to compare the performance of antennas fabricated on

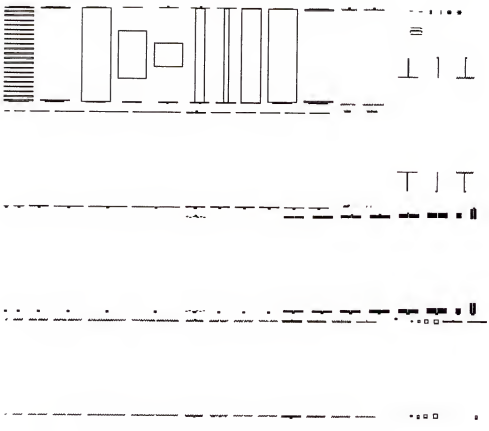


Figure 4-9 Layout of 2nd UF testchip.

almost lossless substrates with that on lossy silicon substrates. The distance between receiving and transmitting antennas is 1 cm for all antenna pairs in this testchip. This testchips include axial length and metal width variation structures for linear, meander, and zigzag dipole antennas, and angle variations between arm elements for zigzag dipole antennas. The axial lengths are 1, 2, 3, 4, and 5 mm, and metal widths are 2.5, 5, 10, 20, and 30 μm. The bend angle between the arm elements of a zigzag dipole antenna is illustrated in

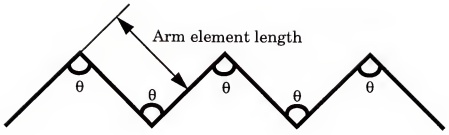


Figure 4-10 Bend angle of a zigzag dipole antenna.

Figure 4-10. Antennas with bend angles of 30, 60, 90, 120, and 150 degree have been included. This testchip also includes interference structures. These structures were designed to estimate interference effects from metal structures between transmitting and receiving antennas on antenna performance. The characterization of these structures were performed by Hyun Yoon and part of the results is reported [Hyu00]. The main purpose for implementing this antenna testchip is to develop optimization strategies of antennas using variables such as length, width, antenna shapes, substrate resistivity, and oxide thickness for wireless interconnection systems.

4.3.4 3rd UF Testchip

The layout of the 3rd UF antenna testchip is shown in Figure 4-11. The size of the chip is similar to the 2nd testchip (4.4 x 4.8 cm^2). Using this design, antennas were fabricated on 10 Ω-cm and 20 Ω-cm silicon, and SOS

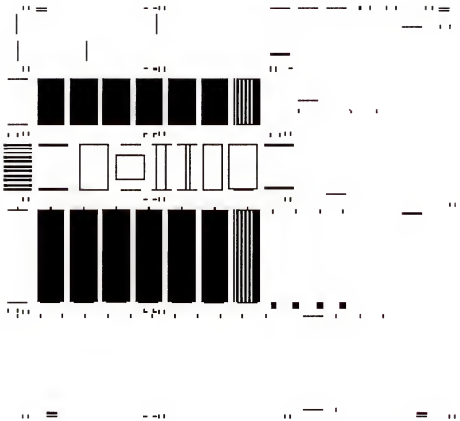


Figure 4-11 Layout of 3rd UF testchip.

substrates. The oxide thickness of the silicon wafers is 3 μm. The testchip includes radiation pattern test structures for a loop antenna, and loop antennas with varying metal widths and radius. It also includes zigzag dipole antennas with 30-degree bend angle, 30-μm metal width, and 2-mm axial length, and interference structures. The distances between receiving and transmitting antennas are 0.5, 1, and 2 cm. The main focus of this testchip was understanding loop antennas. Loop antennas can be a good transmitter

antenna for the wireless interconnection systems because it has an isotropic radiation pattern on the wafer plane.

Table 4-1 summarizes oxide thickness, substrate resistivity, dimensions, and antenna type of the test structures that have been presented in this section.

Table 4-1 Summary of antenna dimensions and substrate type.

Testchip	IBM	UF 1st	UF 2nd	UF 3rd
Substrate	SOS, SOI, Bulk (5 Ωcm)	Bulk (5 Ωcm)	Bulk (10, 20 Ωcm), SOS	Bulk (10, 20 Ωcm), SOS
Antenna length	4 mm, 2 mm	2 mm	1,2,3,4,5 mm	2 mm
Antenna design	Linear	Linear, Meander, Zigzag	Linear, Meander, Zigzag	Loop, zigzag
Oxide thickness	2.4 μm	1.5 μm	1, 3, 9 μm	3 μm
Metal width	1 μm, 4 μm	10 μm	2.5, 5, 10, 20, 30 μm	5, 10, 20, 30 μm

4.4 Antenna Measurement Set-up

4.4.1 Measurement Set-up Using a Vector Network Analyzer

To characterize the on-chip antennas, an antenna measurement set-up which measures S-parameters of antennas was developed [Kim99] and its block diagram is shown in Figure 4-12. The set-up consists of an HP8510C vector network analyzer, a probe station, baluns, and a pair of ground tied signal-signal (SS) probes. 180° hybrid couplers are used as the baluns which reduce the balanced-to-unbalanced mismatch loss. It can be shown that the hybrid coupler can work as a balun even with load impedances other than 50 Ω In general, the input impedances of on-chip antennas are not 50 Ω The analysis of 180° coupler with arbitrary load impedances are described in Appendix B. Use of a balun also helps reducing common-mode noise coupling

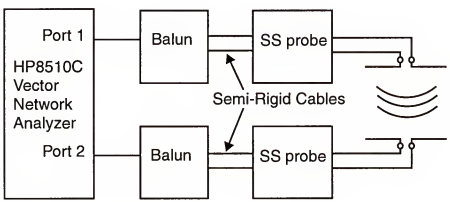


Figure 4-12 Measurement set-up for antenna characterization.

to antennas [Bra00, Meh98]. The signal-signal probes have ground connections near the probe tips. Two pairs of 8-cm long semi-rigid coaxial cables are used for connections between the baluns and signal-signal probes to reduce phase mismatches and to improve the measurement reliability. This set-up is utilized to characterize antennas at frequencies between 6 and 18 GHz.

As stated earlier, this measurement set-up uses microwave-probes to make connections to antennas. The use of probes can introduce errors because the probe tips also can radiate. The situation can be described by using a parallel connection of two 2-port networks between antennas and between probes as shown in Figure 4-13. To de-embed the errors, S-parameters of the open with probes lifted are measured and converted to Y-parame-

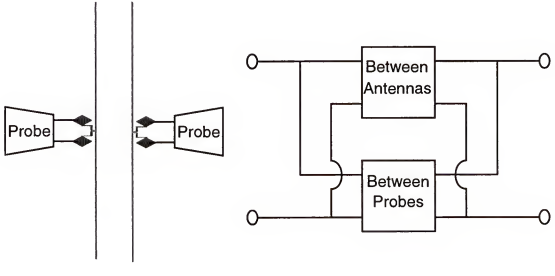


Figure 4-13 Antenna measurement situation using probes.

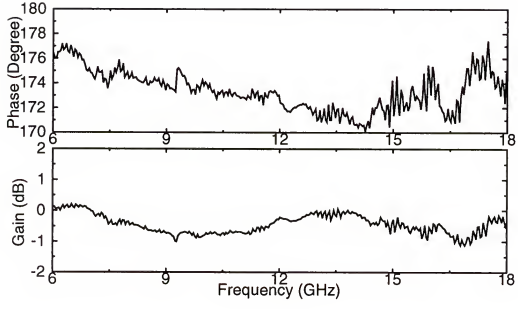
ters. The Y-parameters of the open are subtracted from the Y-parameters of the antennas. S-parameters of the antennas can be computed from the resulting Y-parameters. Use of baluns also can introduce errors because baluns can have phase and amplitude mismatches. The measured phase and gain mismatches of baluns are presented in the next section.

The calibration procedure which is used for S-parameter measurements using baluns and signal-signal probes are the same as the normal full 2-port calibration procedure [HP84]. 50Ω, short, open, and transmission standards are used for the calibration.

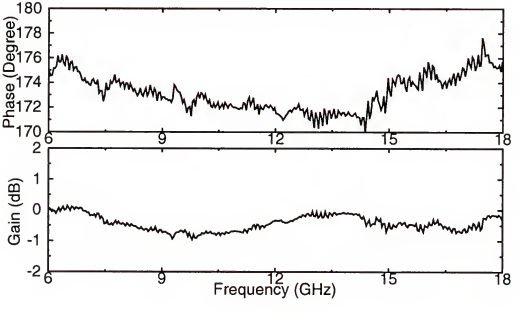
4.4.2 Balun Characterization

In general, the baluns or 180° hybrid couplers have mismatches in phases and amplitudes between the two outputs. Typical specifications of the phase and gain balances are $\pm 10°$ and $\pm 1dB$, respectively. The phase mismatch in this case implies that the phase deviation from the ideal phase difference of 180°. The phase and gain mismatches generate unwanted common mode signals and this will increase mismatch losses and measurement errors. Therefore, it is important to characterize the baluns and make sure that the mismatches are within the specifications, as well as reducing the mismatches.

Figure 4-14 shows the phase and gain mismatch measurement results of baluns which are used in the antenna measurement set-up. In order to measure the mismatches, S_{21} between the Δ port and the one of the output



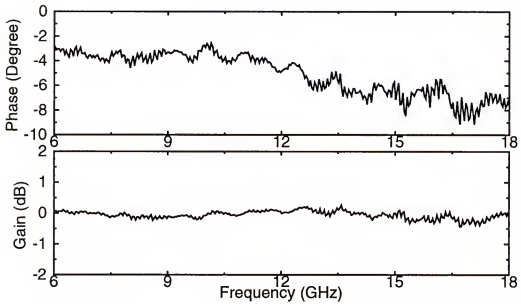
(a)



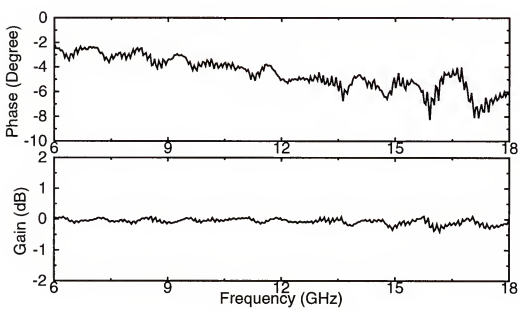
(b)

Figure 4-14 Phase and Gain mismatch measurement for Balun 1 (a) and Balun 2 (b).

port was measured and then S_{21} between the Δ port and the other output port was measured. The Σ port and the output port which is not being measured are terminated with 50 Ω The phase and gain mismatches are computed from the S_{21} measurements. Figure 4-14 (a) shows the maximum phase errors of balun 1 is about -10° and the maximum gain mismatch is about -1 dB in the frequency range of 6 to 18 GHz. Balun 2 shows about the same mismatches as balun 1. The baluns are used with semi-rigid cables connected at the output ports in the measurement set-up. Since the semi-rigid cables are not ideal, they also have mismatches in phases and losses (or gains). The measurement results are shown in Figure 4-15. This shows that the gain mismatches are negligible (less than 0.5 dB). However, the phase mismatches are significant. The maximum measured phase mismatches are about 9°. This phase mismatches can be used to compensate the phase errors of baluns. The measurement results of baluns with semi-rigid cables are shown in Figure 4-16. For this measurement, the semi-rigid cables are connected in a way that the mismatches of the cables compensate the errors of baluns. This measurement shows that the maximum gain mismatches are about the same as in Figure 4-14. However, the maximum phase errors are reduced to about 6°. A comparison of Figure 4-14 and Figure 4-16 reveals that the phase errors of baluns can actually be reduced by properly selecting semi-rigid cables.

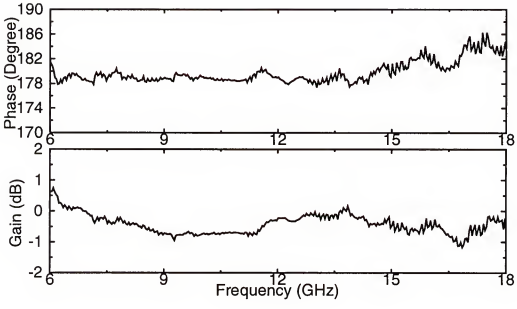


(a)

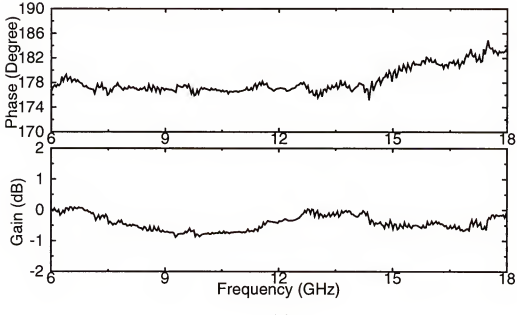


(b)

Figure 4-15 Phase and Gain mismatch measurements between cables A,B (a), and between cables C,D (b).



(a)



(b)

Figure 4-16 Phase and Gain mismatch measurements of Balun1 + cables A, B (a), and Balun2 + cables C, D (b).

4.4.3 Measurements of Semi-rigid Cables Using Balanced and Unbalanced Measurement Set-up

Phases and gains of semi-rigid cables have been measured using balanced and unbalanced (single-ended) measurement set-ups. The characteristic impedance of the semi-rigid cable is 50 Ω and the length is 3 inch. S-parameters of two semi-rigid cables were measured using an unbalanced and balanced measurement set-up. The 180^0 hybrid couplers which has been characterized in 4.4.2 were used in the balanced measurement set-up. Since the balanced measurement requires two same length cables, each of the two cables were measured using the single-ended measurement set-up.

Figure 4-17 shows the gain and phase measurements of the semi-rigid cables. The phase was computed from the measured S-parameters. Figure 4-17 shows that the three measurements have very small differences. These measurements demonstrate that the balanced measurement set-up is working as expected.

The characteristics of a transmission line can be represented by characteristic impedance (Z_0) and propagation constant(β). For a lossless transmission line, the propagation constant is real and can be used to compute the phase velocity. The propagation constant is

$$\beta = \omega\sqrt{LC} = \omega\sqrt{\varepsilon\mu} = \frac{\omega}{c} = \frac{\omega}{v_p} \tag{4.42}$$

where L is a series inductance per length and C is a series capacitance per length. This equation shows that phase velocity of a transmission line is

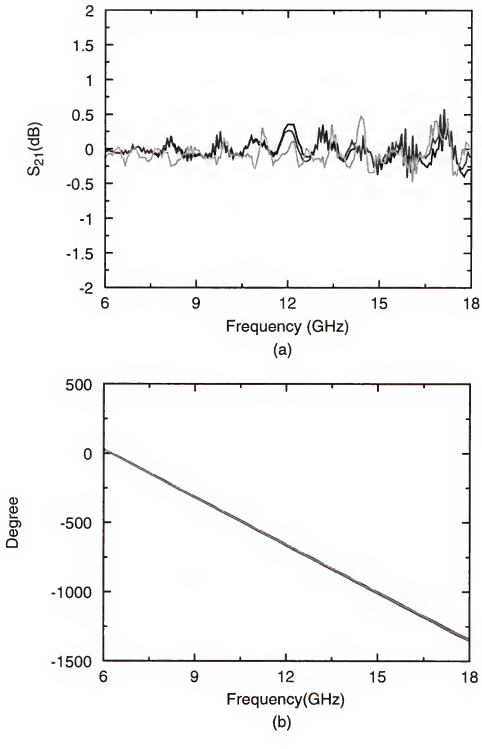


Figure 4-17 Gain (a) and phase (b) measurements of 3-inch long cables using single-ended and balanced measurement set-up.

same as the speed of light in the dielectric which forms the transmission line. The phase delay of a transmission line of length l can be measured using a network analyzer. S_{21} of the transmission line is equal to $e^{-j\beta l}$. Therefore, the phase of S_{21} gives the propagation constant and the phase velocity can be computed using equation (4.42). The computed phase velocity using the phase measurements shown in Figure 4-17 is ~1.7×10^{10} cm/sec, which implies the dielectric constant is ~3.

4.5 Summary

The fundamental antenna parameters were described and the electromagnetic field analyses of short dipole and loop antennas were presented. These give insights in designing on-chip antennas. Linear, meander, and zigzag dipole, and loop antennas were chosen for experimental evaluation based on compactness, and unavailability of the ground plane and lossless substrate in silicon IC's. Antennas were fabricated using the IBM and UF process. The IBM process is a partially scaled 0.1-μm CMOS process. 2-mm and 4-mm linear dipole antennas were implemented on SOI and SOS using this process. To fabricate a wider range of antennas on a large chip, an antenna fabrication process has been developed at UF. The UF process has a single metal layer with no passivation. The process includes oxidation, metal deposition and patterning. Linear, meander, and zigzag dipole, and loop antennas were fabricated on 5 Ω-cm, 10 Ω-cm, and 20 Ω–cm silicon and SOS substrates using the process.

A measurement set-up for integrated antenna characterization has been developed. The measurement set-up uses a network analyzer, baluns, signal-signal probes, and a probe station. 180-degree hybrid couplers are used as baluns. Since dipole antennas are balanced, baluns and signal-signal probes were used to reduce the balanced-to-unbalanced mismatch loss. Baluns and semi-rigid cables were characterized to evaluate the phase errors and gain mismatches. It is shown that the phase errors of balun can be reduced by using phase mismatches of the cables. Semi-rigid cables were measured using balanced and unbalanced measurement set-ups. The measurement shows that the balanced and unbalanced measurements of the semi-rigid cables are very close. This result indicates that the balanced measurement set-up is properly working.

CHAPTER 5
EXPERIMENTAL RESULTS OF ON-CHIP ANTENNAS

5.1 Introduction

Antennas are the largest components in receiver and transmitter circuits. The wireless clock distribution system requires integrated receivers and transmitters including antennas. Therefore, it is critical to evaluate how big an integrated antenna is needed to implement a wireless clock distribution system. As mentioned in Chapter 1, there are two major limitations in integrating compact antennas in silicon ICs. The first is the limit in operating frequency. In the near future, CMOS technology can only support frequencies up to ~20 GHz. Since the antenna efficiency depends on antenna size in terms of wavelength, if there is a limit in operating frequency, there is a limit in reducing the antenna size. This upper operating frequency is expected to be increased above 50 GHz, when CMOS technology scaled below 0.05 μm. The second is from the conductive silicon substrate. Conductivity of silicon substrates reduce the antenna efficiency due to the conduction loss. In order to evaluate the feasibility of integrating antennas, this chapter examines the characteristics of integrated short dipole and loop antennas fabricated on bulk, SOI, and SOS substrates.

5.2 RC Coupling or Wave Propagation

In the measurement of signal transmission gain between two on-chip antennas, the natural question needs to be answered is if the signal transmission occurs through RC coupling or wave propagation.

An RC coupling model for a pair of on-chip dipole antennas is shown in Figure 5-1. C_p's represent the parasitic capacitances of each antenna arm. All the C_p's should have the same values because the areas of antenna arms are all the same. The R's represent substrate resistances between corresponding points under antenna arms. According to this model, it is expected that the signal transmission between the two integrated antennas is lower when the substrate resistivity is high and it is higher when the substrate resistivity is

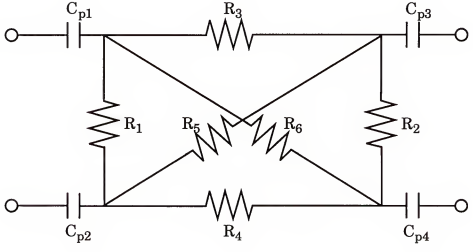


Figure 5-1 RC coupling model for a pair of on-chip dipole antennas.

low. However, the measurement results show the opposite as shown in the following sections. Figure 5-4 and Figure 5-14 show that antenna pairs on SOS have the highest transmission gain and, as the substrate resistivity is reduced, the gain is decreased. Since the substrate resistivity of SOS is almost infinite, the RC coupling should be negligible and the high transmission gains of antenna pairs on SOS cannot be explained using an RC coupling model. In fact, this can be explained using electromagnetic wave propagation. Since the attenuation or conduction loss is increased for electromagnetic wave propagation when the substrate resistivity is lower, antenna pairs on a low resistivity substrate have lower transmission gains. Another evidence which corroborates this is discussed in section 6.3.2. In the section, the antenna transmission gain versus frequency measurements showed dips. Once again, an RC coupling model can not explain the dips in the measurements. The dips in the gain measurement was successfully explained by an addition of two waves traveling through two different wave propagation paths. These results confirm that the signal transmission occurs through wave propagation for on-chip antennas.

5.3 Measurement Results from the IBM Test Structure

5.3.1 Antenna Transmission Gain

Transmission gains of antennas were extracted from S-parameter measurements using the measurement set-up discussed in section 4.3. Since the antennas were measured on a chuck of a probe station and the chuck is

made of a metal, a wooden block was placed between the wafer and the chuck to reduce reflections from the metal chuck. The measurement arrangement is shown in Figure 5-2.

From equation (4.17), S_{21} includes reflection losses at the receiving and transmitting ends. The antenna transmission gains (G_a's) without the reflection losses can be computed using

$$G_a = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} = G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2. \quad (5.1)$$

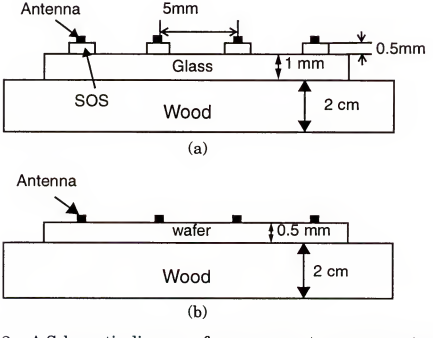


Figure 5-2 A Schematic diagram of measurement arrangements using antennas mounted on a glass slide (a) and antennas on a wafer(b).

The term transmission gain is used in this work to distinguish the gain computed using equation (5.1) from the transducer gain ($|S_{21}|^2$) and antenna gain.

As discussed in section 4.3.1, 2 mm and 4 mm linear dipole antennas were fabricated using the IBM process. S-parameters of linear dipole antennas on bulk, SOI, and SOS wafers were measured and transmission gains were computed [Kim98b]. Figure 5-3 shows antenna transmission gain plots of 4-mm antennas on an SOS substrate. For this measurement, the backside metal layer was removed. The antennas were diced and mounted on a 1-mm thick glass slide. The glass slide was put on a 2-cm thick wooden block (Figure 5-2(a)). The separations between receiving and transmitting antennas

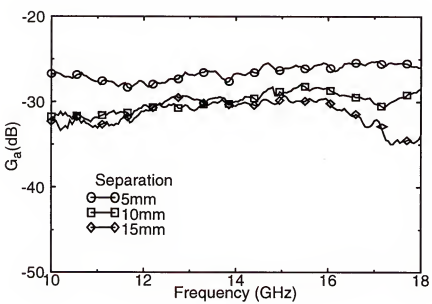


Figure 5-3 Antenna transmission gain measurements of 4-mm antennas on SOS with distances of 5mm, 10mm, and 15mm.

were 5, 10, and 15 mm. The plots show that antenna gains are reasonable (> -35 dB) and decrease with an increasing distance. These measurements confirm signal transmission through radiation since there is negligible capacitive signal coupling through the substrate. For instance, at 15 GHz, the wave lengths in the free space, oxide, silicon and sapphire are 2cm, 1cm, 0.6 cm, and 0.6 cm, respectively. The separation of 1 cm is significantly greater than $\lambda/6$, which means the set-up is measuring intermediate to far fields, where radiation dominates.

Antenna transmission gains of 2-mm long antenna pairs on bulk, SOI, and SOS substrates (with the backside metal layer) are plotted in Figure 5-4. The separation between receiving and transmitting antennas is 4mm (Figure

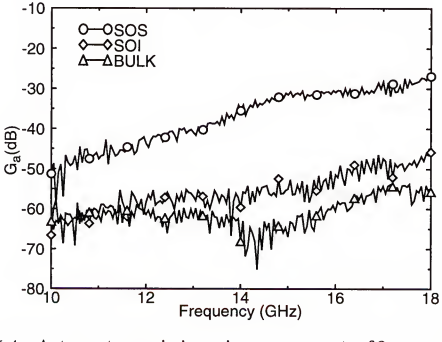


Figure 5-4 Antenna transmission gain measurements of 2-mm antennas on bulk, SOI, and SOS substrates, separated by 4 mm.

5-2(b)). The gain measurements on the SOS substrate confirm signal transmission through wave propagation because the capacitive coupling is negligible. Gains increase with frequency. As expected, gains of an antenna pair on the SOS substrate are higher than those on bulk and SOI substrates. The lower gains of the bulk and SOI antennas are due to the conduction loss in the substrates. The SOS gains are greater than -40 dB at frequencies higher than 13 GHz. The -40-dB corresponds to 15-mV voltage amplitude when a 50-Ω load is attached to the receiving antenna with a 1.5 peak-to-peak driving voltage for the transmitting antenna and perfect matching for both the receiving and transmitting antennas. The similar gain characteristics of antennas on SOI and bulk substrates and the fact that the bulk and SOI gains are lower than those of SOS gains imply that signal transmission is not due to a simple RC coupling even for the antennas on bulk and SOI substrates.

5.3.2 Input Impedance and Circuit Model

The antenna impedance model for dipole antennas shown in Figure 5-5 was suggested by Michael Hamid et al. [Ham97]. This equivalent circuit model is useful for matching network design for receiver and transmitter circuits. Many of the model parameter can be estimated using physical dimensions of the antenna. Since the antenna input impedance includes the radiation impedance, all the model parameters can not be accurately esti-

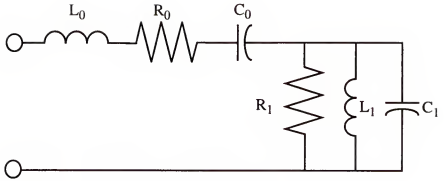


Figure 5-5 On-chip antenna impedance circuit model.

mated. In this study, antenna input impedances were measured and the model parameters were finely adjusted to match the measurement results using the computed parameters as a starting point.

The input impedances of 2-mm linear dipole antennas on SOS, SOI and bulk substrates were computed from S-parameter measurements. The model parameters for the impedance circuit model are shown in Figure 5-5. The measurement and simulation results using the impedance model are compared in Figure 5-6. The plots show good agreement between the measurements and simulations using the model parameters, which indicates that the impedance circuit model is adequate for representing input impedances of integrate antennas. The antennas on SOS substrates have higher reactances than those on bulk and SOI substrates due to lower parasitic capacitance. The plots show that the resonance frequency of the antennas are not

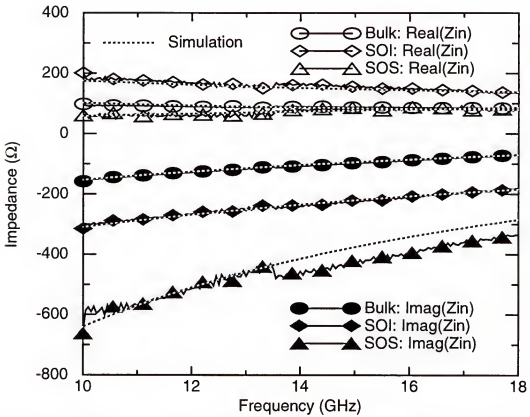


Figure 5-6 Measurement and simulation results of 2 mm linear dipole antenna input impedance.

reached in the measurement frequency range. The resonance can be useful from the matching point of view.

5.4 Measurement Results from the 1st UF Testchip

5.4.1 Antenna Transmission Gain

Antenna transmission gains for linear, meander, and zigzag dipole antennas on bulk wafers were measured [Kim98b]. The testchip was fabricated using the UF process and the layout of the testchip is shown in Figure 4-7. Figure 5-7 shows transmission gains versus distance measurements

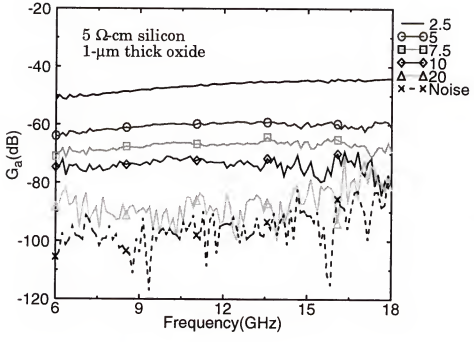


Figure 5-7 Transmission gain measurements of 2mm linear dipole antenna.

plots for pairs of linear dipole antennas. The measurement situation corresponds to the one in Figure 5-2(b). The dotted line in Figure 5-7 shows the background noise level. The background noise level was measured using the signal-signal probes without contacting antennas. It represents the lower limit of the gain measurement for the measurement set-up. The measurements show that when the distance between the transmitting and receiving antennas is increased, the gain is decreased. Transmission gain versus distance plots for linear, meander, and zigzag antenna pairs are shown in Figure 5-8. All three types of antennas show similar transmission gain dependence on distance. Transmission gain of antennas is described by Friis' transmis-

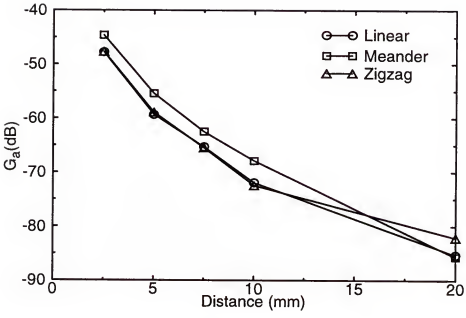


Figure 5-8 Transmission gain versus distance measurements at 10 GHz.

sion formula (4.17). According to the formula, if the distance is increased by a factor of 2, the gain should be decreased by 6 dB. However, the measurements show that the gain reduction is about 10 dB/doubling of the spacing. The zig-zag and linear dipole antennas have approximately the same gain, while the meander dipole antenna has ~3 to 5 dB higher gains.

The gain measurements show that the transmission gain for the all three types of antennas is about -70 dB when the separation is 1 cm. This is too low for a wireless clock distribution system and it is necessary to develop ways to increase the gain.

5.4.2 Input Impedance

Figure 5-9 shows the measured and simulated antenna impedance for the linear, zigzag, and meander dipole antennas on 5 Ω-cm bulk substrates. Once again, the model shown in Figure 5-5 was used, and the model parameters were calculated using the physical dimensions of the antennas and adjusted to match the measurements. The measured and modeled impedances show good match. The linear dipole shows the highest reactance and meander dipole shows the lowest. Only the meander dipole shows the resonance in the measured frequency range (at 18 GHz). For the measured input

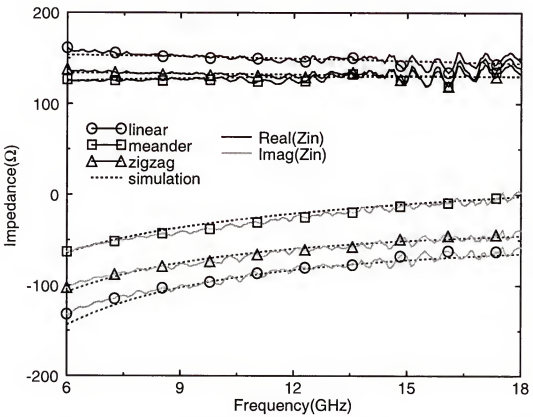


Figure 5-9 Antenna impedance model and impedance measurement and simulation results.

impedances, implementation of integrated matching networks should be straightforward.

5.4.3 Radiation Pattern

Figure 5-10 shows the radiation patterns of linear, zigzag, and meander dipole antennas fabricated on 5 Ω-cm substrates at 10 GHz. The radiation pattern is important in antenna design because it determines the directivity and gain. The placement of receiving antennas should be determined based on the radiation pattern to avoid weak radiation regions. The measured radi-

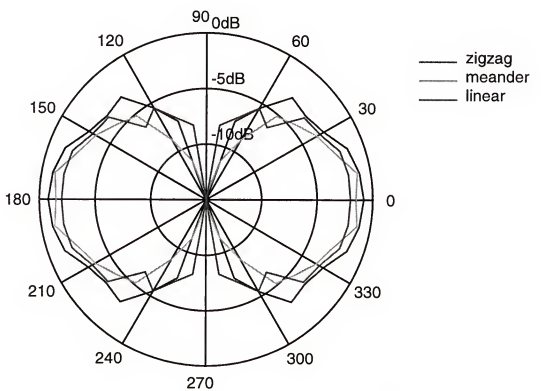


Figure 5-10 Radiation pattern for linear, zigzag, and meander dipole antennas.

ation patterns for the three types on-chip dipole antennas are similar to that of small dipole antennas. The radiation in the axis direction are about 14 dB lower than in the perpendicular direction. This implies that placement of receiving antennas should be avoided in the axis direction of dipole antennas when the antennas are used as a transmitting antenna. These measurement results also show that radiation patterns can be measured using the test structure concept described in section 4.3.2.

5.5 Measurement Results from the 2nd UF Testchip

5.5.1 Antenna Transmission Gain

In order to increase the transmission gains of antennas, and find better antenna structures and substrate types for wireless interconnection, linear, meander, and zigzag dipole antennas with various lengths and widths were fabricated on SOS, and 10 and 20 Ω-cm silicon substrates with an oxide layer with a thickness of 1, 3, and 9 μm. The separation of all the antenna pairs is 1 cm. The testchip is shown in Figure 4-9.

Figure 5-11 shows antenna transmission gain measurements versus axial lengths plot for linear, meander, and zigzag dipole antennas. The antennas were fabricated on a 20 Ω-cm silicon substrate with a 9-μm thick oxide layer (Figure 4-6). The metal width of the antennas is 10 μm. The gains were measured at 15 GHz. The plot shows that 5 mm antennas have ~30 dB higher gain than the 1 mm antennas. The 3-mm antenna pair shows ~16 dB

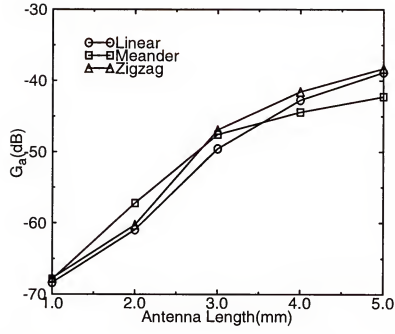


Figure 5-11 Transmission gains versus antenna axial lengths for linear, meander, and zigzag dipole antennas at 15 GHz.

higher gains than the 2-mm antenna pair. This result implies that if a 3-mm antenna is used in a transmitter and a 2-mm antenna is used in a receiver, the gain will be increased by 8 dB compared to the 2-mm antenna pair.

Figure 5-12 shows transmission gain versus metal width measurements. The length of antennas is 2 mm. The plot shows that a 10-dB gain increase can be achieved by changing the width from 2.5 μm to 30 μm. The gain increase comes from lower loss resistance. The lower loss resistance is translated into higher power efficiency. These measurements also show that the gain increase slows when the width is larger than 10 μm due to skin effect. The skin depth of Aluminum at 15 GHz is ~1 μm.

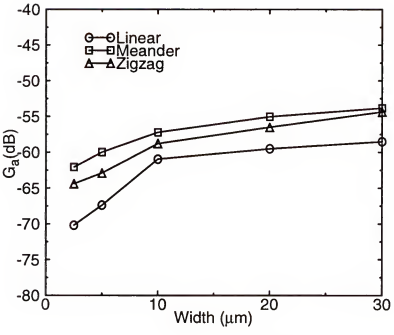


Figure 5-12 Transmission gains versus metal widths for linear, meander, and zigzag dipole antennas.

Figure 5-13 shows a transmission gain versus bend angle plot for zigzag dipole antennas. The metal width and axial length of the antenna is 10 μm and 2 mm, respectively. This measurement shows a pair of zigzag antennas with a bend angle of 30 degree has ~6 dB higher gain than that with a bend angle of 120 degree. When the bend angle is reduced, the actual lengths of the antenna arms are increased. The increase of the arm length increases the current density in the antenna arms. This will, in turn, increase the current vector along the axis of the antenna. This will increase the power density of the radiated electromagnetic field (equation (4.27)). This will increase the transmission gain.

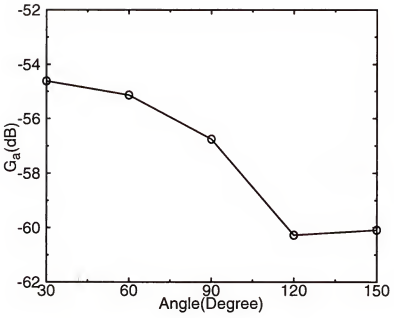


Figure 5-13 Transmission gains versus bend angles of zigzag dipole antennas.

The measurements show that a 2-mm long, and 10-μm wide, 30-degree zigzag dipole antenna has -54 dB gain when the separation is 1 cm. The experimental result using the 1st UF testchip has shown that when the distance is doubled, the gain is reduced by 10 dB for on-chip antennas. This implies that the gain of a zigzag dipole antenna pair will be ~-64 dB when the separation is 2 cm. The metal width experiment shown in Figure 5-12 has shown that the transmission gain will be increased by ~4 dB by changing the metal width from 10 μm to 30 μm. This means that a 2-mm long, 30-μm wide, 30-degree zigzag dipole antenna pair can have transmission gain of ~-50 dB for a separation of 1 cm and ~-60 dB for a separation of 2 cm. This zigzag

dipole antenna pair was fabricated in the 3rd UF test structure and the measurement results are shown in Figure 5-20.

Figure 5-14 shows the gain dependences on substrate resistivities and oxide thicknesses for on-chip antennas. The transmission gains of 2-mm long, 10-μm wide, 120-degree zigzag dipole antenna pairs were measured. The antennas on a 20 Ω-cm substrate show ~7 dB higher gains than the antennas on a 10 Ω-cm substrate, and the antennas on an SOS substrate shows ~25 dB higher gains than the antennas on the 20 Ω-cm substrate. The higher gains of antennas on the SOS substrate is due to the negligible loss associated with

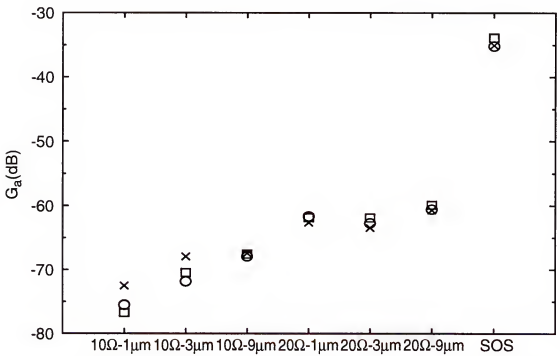


Figure 5-14 Transmission gains versus substrate resistivities and oxide thicknesses of zigzag dipole antenna.

the substrate. This measurement also shows that the oxide thickness doesn't affect the gain much for the antennas on a 20 Ω-cm substrate.

Figure 5-15 shows transmission gains for a linear-linear and a linear-loop antenna pair. Loop antennas are generally considered to have inferior radiation efficiencies compared to dipole antennas. The measurement shows that the linear-loop pair has lower gains at lower frequencies. However, at ~18 GHz, the linear-loop pair shows similar gain as the linear-linear dipole antenna pair. Since loop antennas are more compact than dipole antennas and should have an isotropic radiation pattern on the wafer plane, loop antennas should be more desirable as a transmitter antenna than a dipole antenna. Various loop antennas are implemented in the 3rd UF testchip and the experimental results are presented in section 5.6.

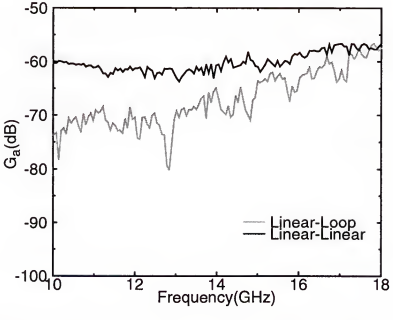


Figure 5-15 Transmission gains of linear-loop and linear-linear dipole antenna pairs.

5.5.2 Input Impedance

The input impedances of linear dipole antennas with various lengths were measured and shown in Figure 5-16. As discussed. the impedance of an on-chip antenna consists of the radiation impedance, loss resistance, and the substrate impedance. The plot shows that the 1-mm antenna has the highest resistance. This high resistance is mostly due to the high substrate resistance associated with the structure. As the lengths of the antennas are increased, the resistances are decreased at low frequencies due to reduced

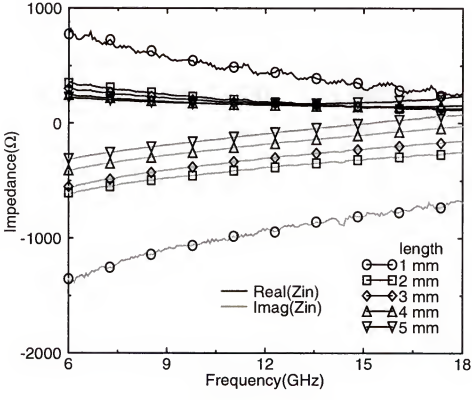


Figure 5-16 Input impedances of linear dipole antennas with various lengths.

substrate resistances. However, at high frequencies, the resistances of the longer antennas are increased. This is due to the increases of the radiation resistances. The 5 mm antenna shows the lowest reactance due to the highest metal-to-substrate parasitic capacitance. The 5-mm antenna shows resonance at ~16 GHz. The design of matching network will be easier for the longer antennas due to lower capacitive reactance which needs to be canceled using an inductor.

Figure 5-17 shows the input impedance of zigzag dipole antennas with various metal widths. The resistance is reduced as the width is increased.

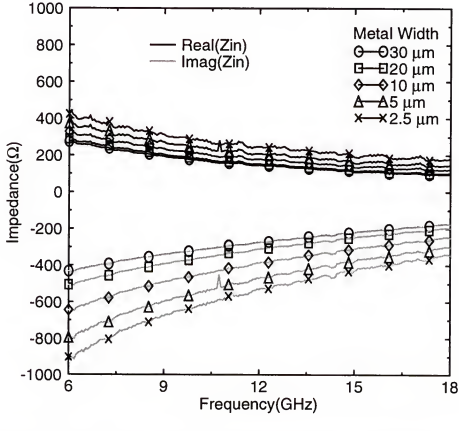


Figure 5-17 Input impedances of zigzag dipole antennas with various metal widths.

When the width is larger than 10 μm, like the antenna gain, the reduction rate is decreased (Figure 5-17), which has been attributed to the skin effect. The plot also shows that the wider antennas have lower reactances due to higher parasitic capacitances.

Figure 5-18 shows the input impedances for zigzag dipole antennas with 5 different bend angles. The metal width of the antennas is 10 μm. The plot shows that the change of the bend angle does not change the resistance much and it mainly changes the reactances of the antenna input impedances. The decrease of the bend angle reduces the reactance due to an increase of parasitic capacitances and inductances of the antenna arms.

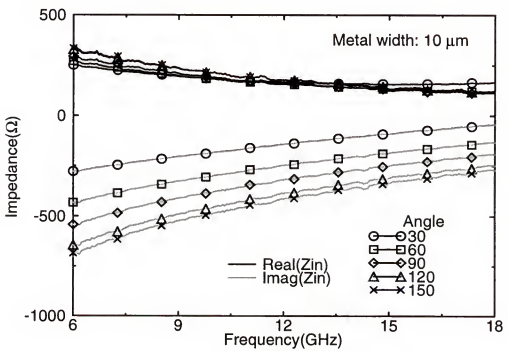


Figure 5-18 Input impedances of zigzag dipole antennas with various bend angles.

Figure 5-19 shows the input impedances of zigzag dipole antennas fabricated on 7 different types of substrates. The impedances were measured at 15 GHz. The antennas were 2-mm long and 10-μm wide with a bend angle of 120 degree. The plot shows that the oxide thickness mainly changes the reactance part of the input impedance while keeping the resistance almost the same. Antennas on 10 Ω-cm substrates show lower resistances than the antennas on 20 Ω-cm substrate due to lower substrate resistances. The substrate resistance is connected in series to the antenna series resistance (R_{loss} + R_r). Therefore, lower substrate resistance reduces the input resistance of the antenna.

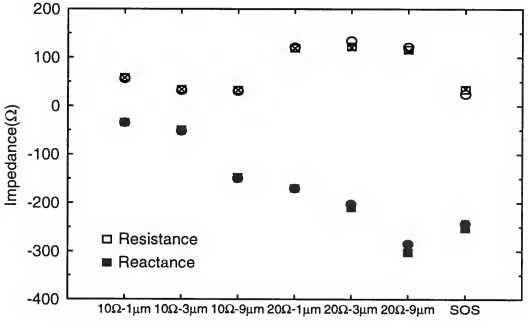


Figure 5-19 Input impedances of zigzag dipole antennas on various substrates.

5.6 Measurement Results from the 3rd UF Testchip

5.6.1 Antenna Transmission Gain

Two pairs of 2-mm long, 30-μm wide, 30 degree zigzag dipole antennas were fabricated in the 3rd UF testchip. One pair was separated by 1 cm and the other was separated by 2 cm. The antennas were fabricated on 20 Ω-cm silicon wafers.

As predicted from the results of the 1st and 2nd UF testchips, the transmission gain of the antenna pairs with separations of 1 cm and 2 cm are ~-50 dB and ~-60 dB at 15 GHz. The maximum gains are -45 dB and -56 dB near 18 GHz for the pairs with separations of 1 cm and 2 cm respectively. The

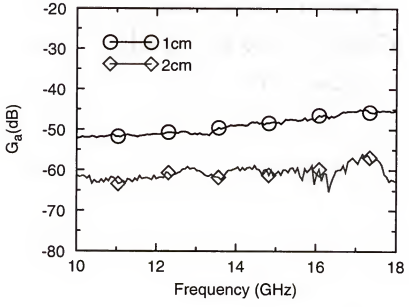


Figure 5-20 Transmission gain of 2 mm long, 30 μm wide, 30 degree zig-zag dipole antennas separated by 1 cm and 2 cm.

measurements thus far have shown that the gains in general increase with frequency, and it should be possible to increase even further by increasing the operating frequencies.

Figure 5-21 shows transmission gains of loop antennas for varying metal widths. The diameter of the loop antenna is 200 μm and the antennas were fabricated on 20 Ω-cm silicon substrates with a 3-μm oxide layer. The metal widths are 5, 10, 20, 30, and 40 μm. The layout of the loop antenna test structures are shown in Figure 5-22. The test structures consist of a loop and a zigzag dipole antenna separated by 1 cm. The zigzag dipole antenna is 2-mm long and 30-μm wide, and has 30-degree bend angle. The transmission

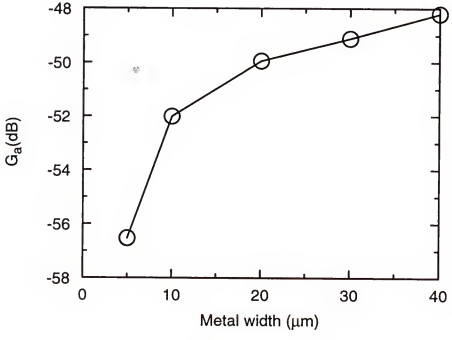


Figure 5-21 Transmission gains of 200-μm loop antennas with 5 metal widths at 15 GHz.

Figure 5-22 A layout of a loop-zigzag dipole antenna pair.

gains were measured at 15 GHz. Figure 5-21 shows that the gain can be increased by ~8 dB by increasing the metal width from 5 μm to 40 μm. Like the dipole antenna results shown in Figure 5-12, the gain increase slows when the width becomes larger than 10 μm due to the skin effect. This plot shows that a loop-zigzag dipole antenna pair can have transmission gain of ~-50 dB at 15 GHz. This gain is similar to that of a zigzag dipole antenna pair shown in Figure 5-20, which suggests that loop antennas can be a good transmitter antenna when they are used with zigzag dipole receiving antennas.

To estimate substrate effects on the loop antenna performances, the 3rd UF testchip was fabricated on an SOS substrate, and 20 Ω-cm and 10 Ω-cm silicon wafers. The transmission gain versus frequency plots of the antennas are shown in Figure 5-23. For this measurement, the loop and zigzag dipole antenna pair shown in Figure 5-22 has been utilized. The loop-zigzag

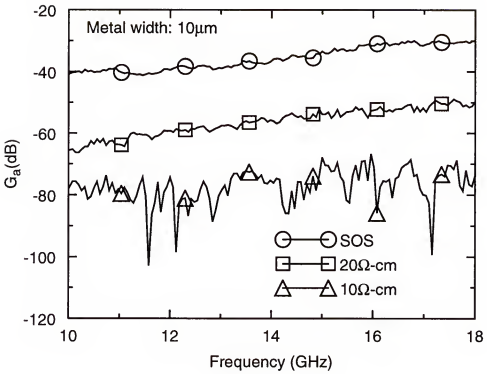


Figure 5-23 Transmission gains of 200-μm loop antennas on SOS, and 20Ω-cm and 10Ω-cm silicon substrates.

pair on the SOS substrate shows the highest gain. The maximum gain in the measured frequency range is ~-30 dB. The antenna pair on a 20 Ω-cm silicon substrate shows about 20 dB lower gain than those on the SOS wafer. The maximum gain is ~-50 dB. The plot shows that the gains almost monotonically increase between 10 and 18 GHz. It may be possible to get higher gains at higher frequencies. The loop zigzag pair on a 10 Ω-cm substrate shows gains below -70 dB. The gain plot is noisy due to the low gain.

The required maximum separation between on-chip antennas for the wireless interconnection system is 2 cm. Figure 5-24 shows the transmission gains of a loop-zigzag dipole antenna pair on a 20 Ω-cm silicon substrate with separations of 1cm and 2cm. The loop antenna has a diameter of 200 μm and metal width of 30 μm. The zigzag dipole antenna is the same as the one in Figure 5-22. The maximum transmission gain at the 1-cm separation is ~-48dB and at the 2-cm separation pair is ~-60 dB near 18 GHz. These gains are ~4dB less than those of the zigzag dipole antenna pairs shown in Figure 5-20.

It has been shown that a clock receiver can lock to the transmitter when the path loss between the receiving and transmitting antennas is -64

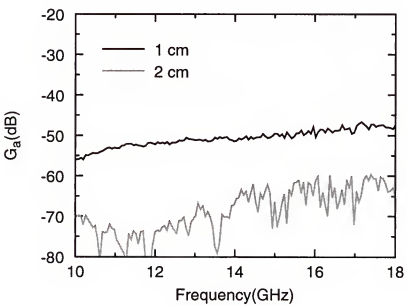


Figure 5-24 Transmission gain of loop-zigzag dipole antenna pairs with separations of 1 cm and 2 cm.

dB [Flo00]. Therefore, to lock, the transmission gain of -60 dB is sufficient. Even though the loop-zigzag antenna pair has lower gains than the zigzag dipole antenna pair, since the loop antenna is much smaller and has an isotropic radiation pattern, the loop antenna can still be a better transmitter antenna structure for wireless interconnection.

5.6.2 Input Impedance

The input impedance of a 2-mm long, 30-μm wide, 30 degree zigzag dipole antenna on a 20 Ω-cm substrate is shown in Figure 5-25. The resistance is 70 to 110 Ω and the reactance is -140 to -70 Ω in the frequency range

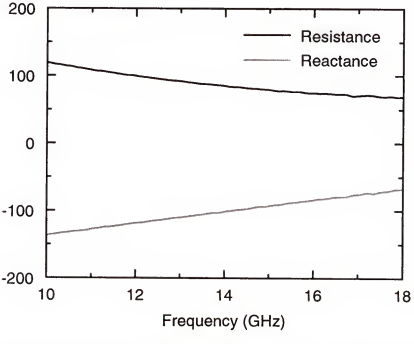


Figure 5-25 Input impedance of 2-mm long, 30-μm wide, 30 degree zigzag dipole antenna on a 20 Ω-cm silicon substrate.

between 10 and 18 GHz. Once again, it should be easy to implement a matching network for this impedance.

Figure 5-26 shows input impedances of loop antennas with varying metal widths. The input impedances are inductive. Inductive input impedance is good for matching network design in receiver circuits, because the receiver antenna is connected to an LNA and the input impedances of LNAs are generally capacitive. The plot shows that the increase of metal width decreases both resistance and reactance. The reduction in the resistance comes from a decrease in the metal loss resistance and the reduction in the

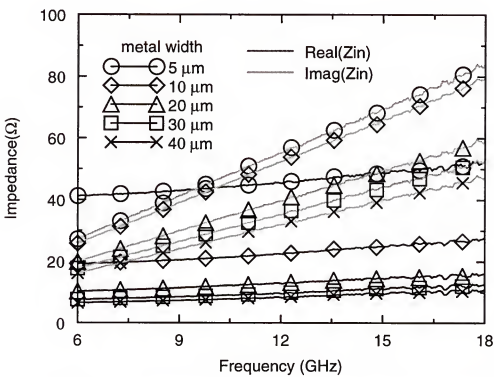


Figure 5-26 Input impedances of 200-μm loop antennas with 5 metal widths.

reactance comes from the increase of parasitic capacitances and decrease of inductance (see section 2.2.2).

5.6.3 Radiation Pattern

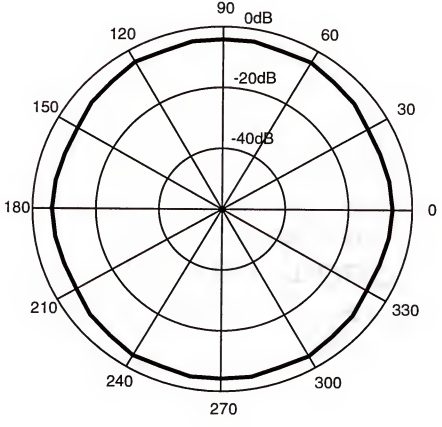
The radiation pattern of the loop antenna was measured. Since integrated antennas can not be rotated once fabricated, loop antennas with specific angles were fabricated as shown in Figure 5-27(a). The loop diameter is 200 μm and the metal width is 10 μm. The receiving antennas were zigzag dipole antennas. Since the loop is symmetric on the substrate plane, the radiation pattern is expected to be isotropic on the substrate plane. Figure 5-27(b) shows an almost ideal isotropic radiation pattern. This isotropic radiation pattern is a desirable characteristic for a transmitting antenna, because it eliminates the restrictions on placement of receiving antennas.

5.7 Summary

Integrated antennas were implemented on bulk, SOI, and SOS substrates. Linear, meander, and zigzag dipole, and loop antennas have been implemented and experimentally evaluated.

Antenna transmission gains, radiation patterns, and input impedances for linear, meander, and zigzag dipole, and loop antennas were measured. In order to develop optimization strategies for antennas, antennas with varying metal widths, lengths, and bend angles were implemented and studied. The transmission gain measurement shows that a 5-mm long dipole

(a)



(b)

Figure 5-27 Layout of radiation pattern test structure (a) and radiation pattern measurement for a loop antenna.

antenna pair has ~30 dB higher gains than a 1-mm antenna pair and a ~10 dB gain increase can be achieved by increasing the metal widths of the antennas from 2.5 to 10 μm. A change of the bend angle of a zigzag dipole antenna also can increase gain. A 30-degree antenna pair shows ~6 dB higher gain than a 120 degree antenna pair. Loop antennas show similar gain dependence on the metal width as dipole antennas. Gain dependence on the distance between receiving and transmitting antennas were measured. The measurement show that the gain is decreased by ~10 dB when the distance is increased by a factor of 2.

To estimate the impact of the substrate type on antenna characteristics, antennas were fabricated on an SOS substrate, and 10 and 20 Ω–cm silicon substrate with an oxide layer thickness of 1, 3, and 9 μm. Antennas on the SOS substrate have ~25 dB higher gain than the antennas on 20 Ω–cm. This measurement indicates that the power transmission between receiving and transmitting antenna occurs through radiation rather than RC coupling because the resistive and capacitive coupling should be negligible in an SOS substrate. Antennas on a 20 Ω–cm substrate show ~7 dB higher gain than the antennas on a 10 Ω–cm substrate. Changing oxide thickness modifies the input impedances of antennas. The input impedances of the antennas have been modeled using a previously reported circuit model. The measurement results and the simulation results using the impedance model match well. Radiation patterns for the dipole and loop antennas were measured. The

radiation patterns of the dipole antennas are similar to that for a short dipole antenna and the loop antenna exhibits an isotropic radiation pattern.

2-mm long, 30-μm, wide, 30-degree zigzag dipole antenna pairs were implemented on a 20 Ω–cm silicon substrate. The transmission gains at separations of 1 cm and 2 cm are -45 dB and -56 dB near 18 GHz. A loop-zigzag dipole pair can have gains comparable to those of a zigzag dipole pair (~4 dB less for the loop-zigzag pair). The loop-zigzag pair shows -60dB of gain for a separation of 2 cm. The -60 dB is sufficient to lock to a transmitted clock signal. With an isotropic radiation pattern and compact size, the loop antenna is ideal as a transmitter antenna.

Through the experiments, in the absence of interfering structures, it has been shown that the signal transmission and reception using on-chip antennas is possible in an area of 2-cm radius. The experimental results confirm signal transmission through radiation. This work suggests that on-chip radio communication using integrated antennas is feasible.

CHAPTER 6
PROPAGATION OF ELECTROMAGNETIC WAVES FROM AN ON-CHIP ANTENNA

6.1 Introduction

To understand the propagation of electromagnetic waves from on-chip antennas, it is important to know the wave propagation paths. When electromagnetic waves are traveling predominantly through one medium, phase velocity measurements can show which medium the wave is traveling. If there are multiple wave propagation paths, then both experimental and theoretical investigations are necessary to determine the wave propagation paths. This chapter presents the results of a theoretical and an experimental study to determine the paths of electromagnetic waves which an on-chip antenna pair uses to communicate.

6.2 Wave Propagation in a Three Layered Medium

Some of the measurement situations of on-chip antennas can be represented by an antenna in a three layered medium. For example, the first region could be air, the second region could be oxide or sapphire, and the third region could be a conductive silicon substrate or a metal plate. This section introduces the theoretical electromagnetic field analysis of a simplified

case and shows the measurement results corresponding to the simplified case.

6.2.1 Theoretical Analysis

The theoretical electromagnetic field analysis of the on-chip antenna is prohibitively difficult. However, the analysis of a simplified case is possible and performed by King [Kin92a]. A schematic diagram of a Hertzian dipole in a three layered medium is shown in Figure 6-1. In the analysis, the antenna is assumed to be a Hertzian dipole, the dielectric layer is assumed to be electrically thin, and the wave numbers satisfy the inequalities in equations (6.1) and (6.2).

$$k_0^2 l^2 \ll k_1^2 l^2 \ll 1 \tag{6.1}$$

$$k_0^2 \ll k_1^2 \ll |k_2|^2 \tag{6.2}$$

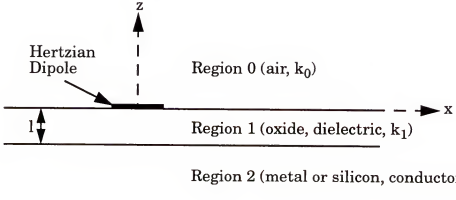


Figure 6-1 Hertzian dipole on dielectric in a three-layered region.

Region 0 (air) and region 2 (metal or silicon) are assumed to be semi-infinite.

A detailed analysis can be found in Appendix C. The electric and magnetic fields generated by a Hertzian dipole antenna in Figure 6-1 are

$$E_{0\rho}(\rho, \phi, z) = \frac{\omega\mu_0}{4\pi k_0} \tag{6.3}$$

$$\cos\phi\left[2e^{ik_0 r}\left\{\varepsilon\left(\frac{z}{r}\right)\left(\frac{ik_0}{r}-\frac{1}{r^2}\right)-\varepsilon^2\left[\frac{ik_0}{r}-\frac{1}{r^2}-\frac{i}{k_0 r^3}-k_0^2\varepsilon\left(\frac{r}{\rho}\right)\left(\frac{\pi}{k_0 r}\right)^{\frac{1}{2}}e^{-iP_2}\Im(P_2)\right]\right\}\right]$$

$$E_{0\phi}(\rho, \phi, z) = -\frac{\omega\mu_0}{4\pi k_0}\sin\phi\left[2e^{ik_0 r}\left\{\varepsilon\left(\frac{z}{r}\right)\left(\frac{ik_0}{r}-\frac{1}{r^2}\right)\right.\right. \tag{6.4}$$

$$\left.\left.-\varepsilon^2\left[\frac{2}{r^2}+\frac{2i}{k_0 r^3}+\left(\frac{z}{r}\right)^2\left(\frac{ik_0}{r}-\frac{3}{r^2}-\frac{3i}{k_0 r^3}\right)+ik_0\varepsilon\left(\frac{r^2}{\rho^3}\right)\left(\frac{\pi}{k_0 r}\right)^{\frac{1}{2}}e^{-iP_2}\Im(P_2)\right]\right\}\right]$$

$$E_{0z}(\rho, \phi, z) = -\frac{\omega\mu_0}{4\pi k_0}\cos\phi\left[2\varepsilon e^{ik_0 r}\left\{\left(\frac{\rho}{r}\right)\left(\frac{ik_0}{r}-\frac{1}{r^2}\right)-k_0^2\varepsilon\left(\frac{\pi}{k_0 r}\right)^{\frac{1}{2}}e^{-iP_2}\Im(P_2)\right\}\right] \tag{6.5}$$

$$B_{0\rho}(\rho, \phi, z) \tag{6.6}$$

$$= \frac{\mu_0}{4\pi}\sin\phi\left[2\varepsilon e^{ik_0 r}\left\{\frac{2}{r^2}+\frac{2i}{k_0 r^3}+\left(\frac{z}{r}\right)^2\left(\frac{ik_0}{r}-\frac{3}{r^2}-\frac{3i}{k_0 r^3}\right)+ik_0\varepsilon\left(\frac{r^2}{\rho^3}\right)\left(\frac{\pi}{k_0 r}\right)^{\frac{1}{2}}e^{-iP_2}\Im(P_2)\right\}\right]$$

$$B_{0\phi}(\rho,\phi,z) = \frac{\mu_0}{4\pi}\cos\phi\left[2\varepsilon e^{ik_0 r}\left\{\frac{ik_0}{r}-\frac{1}{r^2}-\frac{i}{k_0 r^3}-k_0^2\varepsilon\left(\frac{r}{\rho}\right)\left(\frac{\pi}{k_0 r}\right)^{\frac{1}{2}}e^{-iP_2}\Im(P_2)\right\}\right] \tag{6.7}$$

$$B_{0z}(\rho,\phi,z) = -\frac{\mu_0}{4\pi}\sin\phi \tag{6.8}$$

$$\left[2e^{ik_0 r}\left\{\varepsilon\left(\frac{z}{\rho}\right)\left(\frac{ik_0}{r}-\frac{3}{r^2}-\frac{3i}{k_0 r^3}\right)-\varepsilon^2\left(\frac{\rho}{r}\right)\left[\frac{1}{r^2}+\frac{3i}{k_0 r^3}-\frac{3}{k_0^2 r^4}+\left(\frac{z}{r}\right)^2\left(\frac{ik_0}{r}-\frac{6}{r^2}-\frac{15i}{k_0 r^3}\right)\right]\right\}\right]$$

In these equations,

$$r=[\rho^2+z^2]^{1/2} \tag{6.9}$$

$$\varepsilon = \frac{\left(\frac{k_0}{k_2}\right)-ik_0 l}{1-\frac{ik_1^2}{k_2}} \tag{6.10}$$

$$P_2 = \frac{k_0 r}{2}\left(\frac{\varepsilon r+z}{\rho}\right)^2 \tag{6.11}$$

$$\Im(P_2) = \frac{1}{2}(1+i)-\int_0^{P_2}\frac{e^{it}}{\sqrt{2\pi t}}dt \tag{6.12}$$

The integral in $\Im(P_2)$ is the well-known Fresnel integral.

From the above equations, electromagnetic field components can be computed using a mathematical software package such as Maple [Map91]. Phase velocity of the wave can be computed from the phase of the electromagnetic field components.

Figure 6-2 shows the computed phase delay of the electric field from a Hertzian dipole antenna on an SOS substrate. The SOS substrate (region 1)

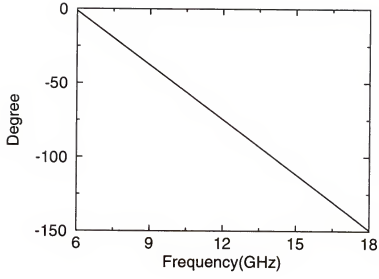


Figure 6-2 Phase delay simulation result of Hertzian dipole antenna on SOS on metal plate.

is assumed to be 0.5-mm thick and on a metal plate. The distance of the field point on the wafer surface from the antenna is 1 cm. This situation satisfies the inequalities ((6.1), (6.2)) used to derive the expressions. The phase velocity of the electromagnetic wave can be computed from the slope of the plot and the computed velocity is ~$3x10^{10}$ cm/sec. A further simulation study reveals that when the thickness of the dielectric layer and the frequency are increased such that the thickness of the dielectric becomes greater than ~$\lambda/4$, the phase velocity is reduced [Att51]. When the thickness of the dielectric is close to a wavelength, the velocity becomes that of the dielectric. When the thickness of the dielectric is very small compared to a wavelength, the phase velocity is close to the speed of light in the air ($3x10^{10}$ cm/sec). The case of the

dipole antennas on silicon wafers should also be similar to this case, because the thickness of the oxide layer is very thin (1~9 μm) compared to a wavelength (~1 cm).

Using the expressions in (6.3)~(6.8), Poynting vector can be computed from

$$\bar{S} = Real(\bar{E} \times \bar{H}^*) \tag{6.13}$$

From the magnitude of the Poynting vector, the radiation pattern of an antenna can be plotted. Since the antenna used to analyze the electromagnetic fields is a Hertzian dipole antenna, the actual radiation pattern of the on-chip dipole antenna may be different. However, this pattern should give a qualitative understanding of the radiation characteristics of the on-chip dipole antennas. Figure 6-3 shows the radiation pattern plot. The plot shows the radiation pattern in the y-z plane (ϕ=90°) in Figure 6-1. The region 2 is assumed to be a 20 Ω-cm silicon substrate and region 1 is assumed to be a 3-μm thick oxide layer. The plot shows that power propagation along the wafer surface is inefficient. It is about 40 dB less than that in the z-direction.

6.2.2 Experimental Results

The speed of EM wave can be estimated using a phase delay measurement between the receiving and transmitting antennas. The phase delay between two on-chip antennas can be approximated as

$$\phi(\omega) \cong \frac{\omega l}{c_1} + \phi_Z(\omega)\,. \tag{6.14}$$

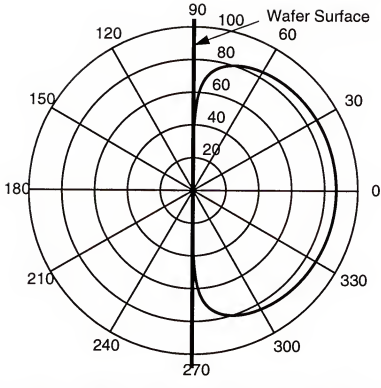


Figure 6-3 Radiation pattern of a Hertzian dipole antenna on silicon substrate.

The first term comes from the distance between the receiving and transmitting antennas. The second term is associated with the phase delay of the antenna input impedance. Since the second term is fixed for a given antenna structure and at a given frequency, if the phase delays are measured for several antenna separations and subtracted from each other, the speed of electromagnetic wave can be obtained using the following equations

$$\phi_n - \phi_m = \frac{\omega}{c_1}(l_n - l_m). \tag{6.15}$$

$$c_1 = \frac{\omega(l_n - l_m)}{\phi_n - \phi_m} \tag{6.16}$$

If we plot the phase differences as a function of frequency, the phase difference should show linear dependence on frequency and the speed of electromagnetic wave can be computed from the slope of the phase differences.

Figure 6-4 shows the phase difference of zigzag dipole pairs on an SOS substrate on a metal plate. The length of the zigzag dipole antenna is 2 mm. Antenna pairs with a separation of 2.5 mm and 5 mm between the receiving and transmitting antennas were fabricated and the phase delays were measured. The plot shows the difference of the phase delays of the two pairs. The phase velocity computed using equation (6.16) is ~2.9×10^{10} cm/sec. This result is close to the predicted value using King's formula discussed in the previous section. In this case, the wave travels through the air. This wave is

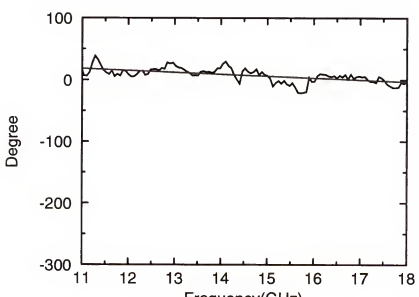


Figure 6-4 Measured phase difference plot of zigzag dipole antenna on SOS on metal plate

called surface wave. When the dielectric layer is electrically thin, the phase velocity is that in the air.

6.3 Propagation of Electromagnetic Waves from an On-chip Antenna

6.3.1 Possible Ways of Wave Propagation

There are several possible electromagnetic wave propagation paths between two on-chip antennas. Figure 6-5 shows a schematic diagram of the possible wave propagation paths. The figure shows four wave paths (path A, B, C, D). The figure depicts the antenna measurement situation when a silicon wafer with integrated antennas is on a glass layer, a wood block or air. To

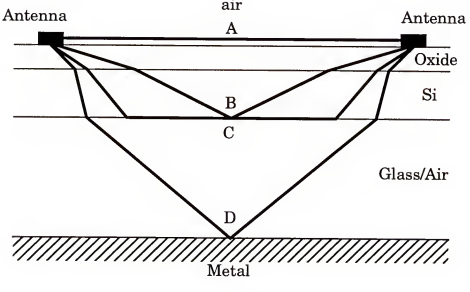


Figure 6-5 Possible wave propagation paths between two on-chip antennas.

have an air gap between the wafer and the metal plate, the wafer can be supported by glass blocks at the edges of the wafer.

Path A represents a direct wave transmission between the two antennas. The wave in this path travels through both air and the oxide layer and is called surface wave. To make sure the tangential fields are continuous across the boundary, the wave going through air and the wave going through the oxide should have the same phase velocity [Att51, Rei79]. The phase velocity of the surface wave is bounded by the speed of the light in air (on the higher end) and in the oxide (on the lower end). When the oxide thickness is electrically thick ($> \lambda/4$), the phase velocity of the surface wave is close to that in the oxide, and when the thickness is electrically thin, the velocity is close to that in the air [Att51]. For on-chip antennas, the oxide thickness is very thin (~3 μm) compared to the wavelength (~1 cm). Therefore, the phase velocity of the wave going through path A should be close to that in the air ($3x10^{10}$ cm/sec). The surface wave suffers attenuation due to the conductivity of the silicon. The situation is similar to the ground-wave propagation [Jor68]. The attenuation depends on distance, frequency, and conductivity of the silicon substrate. The electric field of the surface wave can be represented as

$$\overline{E}_{surface} = \overline{E} e^{-j\beta R} \frac{A}{R}. \tag{6.17}$$

In this equation, R is the distance and A is the attenuation factor. A can be approximated as

$$A \cong e^{-\alpha_{surf} R}, \tag{6.18}$$

where α is the attenuation coefficient of the surface wave. The attenuation factor A can be estimated from the measurement data of on-chip antennas on a metal plate. By putting the wafer with integrated antennas directly on a metal plate, the path C and path D can be eliminated. Path B can be ignored because of severe attenuation through the silicon substrate. If transmission gains of on-chip antenna pairs on a metal plate with two different distances are measured, then the ratio of the transmission gains is

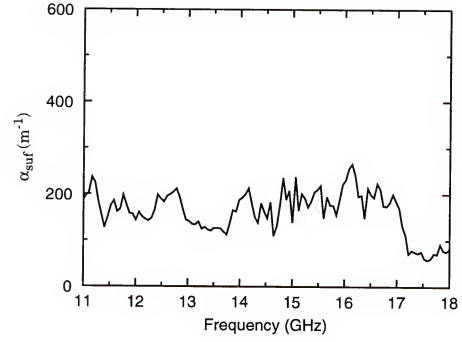
$$\frac{G_a(R_1)}{G_a(R_2)} = \frac{\left|\bar{E}_{surface}(R_1)\right|^2}{\left|\bar{E}_{surface}(R_2)\right|^2} = \left(\frac{R_2}{R_1}\right)^2 e^{-2\alpha_{suf}(R_1 - R_2)} \tag{6.19}$$

G_a is defined in chapter 5. The attenuation coefficient α_{suf} can be estimated using the following equation.

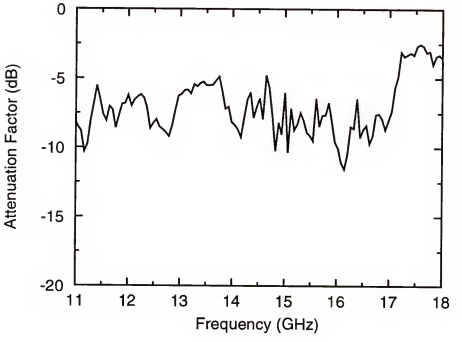
$$\alpha_{suf} = \frac{20\log\left(\frac{R_2}{R_1}\right) + G_a(R_2) - G_a(R_1)}{20(R_1 - R_2)\log(e)} \tag{6.20}$$

Figure 6-6 shows the estimated α_{suf} from measured data and the computed attenuation factor. For the estimation, antennas on a 10 Ω-cm silicon substrate were measured. The separations of the measured antenna pairs are 2.5 mm and 5 mm. The plot shows that the attenuation is ~7 dB for the antennas on the 10 Ω-cm substrate for a 5-mm separation.

Path B represents the wave path going through the silicon substrate and reflecting back at the interface between the silicon and the glass or air to reach the receiving antenna. Since the thickness of the oxide (~3 μm) is negligible compared to that of silicon (~0.5 mm), the electromagnetic wave going



(a)



(b)

Figure 6-6 Measured α (a) and the computed attenuation factor for 5-mm distance (b).

through this path is mostly going through the silicon substrate. Therefore, the wave going through path B suffers a lot of loss (greater than 40dB for 1 cm distance in 10 Ω-cm silicon) and the contribution of this wave to the total transmission is negligible. Path B can be ignored in most cases except when the resistivity of the silicon is high (> 40 Ω-cm).

Path C represents the wave path going through the silicon substrate and the back surface of the silicon wafer. The wave going through this path is called a lateral wave. The lateral wave has been studied and summarized by Tamir [Boa82]. A lateral wave is generated by a beam of finite extent incident at an angle close to the critical angle. The generation of the lateral wave is associated with the total reflection. The finite extent of the incident field is instrumental in producing the lateral wave and the lateral wave cannot exist if the incident wave is an infinite plane wave. The generation of the lateral wave field can be explained qualitatively using Figure 6-7. In the figure, the refractive index of medium 1 is assumed to be higher than that of medium 2 ($n_1 > n_2$). When a ray I in the medium 1 is incident on the interface of the two media with an incident angle θ_1, the reflected ray B and refracted ray C with an angle θ_2 are generated, as shown in Figure 6-7 (a). If a ray I′ is incident from the medium 2 with an angle θ_2, then it generates the reflected ray C and refracted ray B with an angle θ_1. If the incident angle of the ray I in the medium 1 is increased so as to reach the critical angle (θ_c), then the refracted angle becomes 90°, as shown in Figure 6-7 (b). As in the case shown in Figure 6-7 (a), if a ray in the medium 2 is incident on the interface with 90° incident

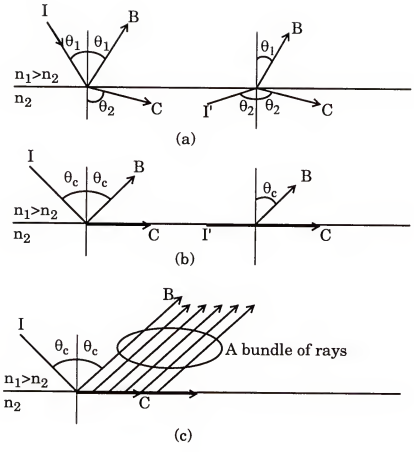


Figure 6-7 Generation of a lateral wave by using ray concepts. (a) At left, a ray I incident at an angle $\theta_1<\theta_c$ produces reflected ray B and refracted ray C; at right, the reciprocal case, a ray I' incident at the angle θ_2 produces a reflected ray C and refracted ray B. (b) When $\theta_1=\theta_c$. (c) A bundle of rays showing the lateral wave field.

angle (i.e. a ray travels just below and parallel to the interface), then it will generate a refracted ray with an angle equal to the critical angle. Since the refracted ray C from an incident ray I can be regarded as an incident ray with an incident angle 90^o in medium 2, the incident ray I produces a bundle of rays which form a lateral wave field, as shown in Figure 6-7 (c).

Figure 6-8 shows a detailed diagram of wave propagation in path C. Since the dielectric constant of silicon is higher than that of glass or air, if the incident angle (θ_2) in the silicon is equal to the critical angle(θ_{2c}), total reflection occurs at the boundary and the wave travels along the surface. The critical angle is 17 degree for the air and silicon interface and it is 37 degree for the glass and silicon assuming the dielectric constant of glass is 4.3 and that of silicon is 11.7. The wave travel along the surface will return back into the silicon substrate with the critical angle and reach the receiving antenna.

The wave traveling through path C suffers from three different attenuation mechanisms. The first is from transmission coefficients t_{12} and t_{21}. The transmission coefficients of the electric field for a TE mode is expressed as follows

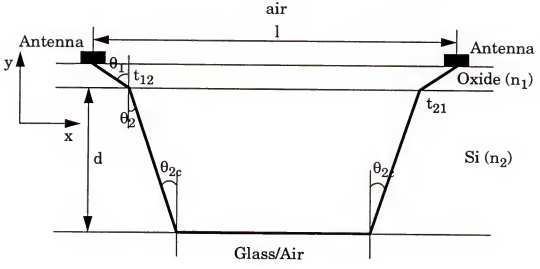


Figure 6-8 A detailed diagram of wave propagation in path C.

$$t_{12} = \frac{2n_1\cos\theta_1}{n_1\cos\theta_1 + \hat{n}_2\cos\hat{\theta}_2} \tag{6.21}$$

$$t_{21} = \frac{2\hat{n}_2\cos\hat{\theta}_2}{n_1\cos\theta_1 + \hat{n}_2\cos\hat{\theta}_2} \tag{6.22}$$

The power transmission coefficient is

$$T = \frac{4n_1\hat{n}_2\cos\theta_1\cos\hat{\theta}_2}{(n_1\cos\theta_1 + \hat{n}_2\cos\hat{\theta}_2)^2} \tag{6.23}$$

where n_1 and $\hat{n}_2$ are indices of refraction of oxide and silicon, respectively. Since the silicon substrate is conductive, the index of refraction is complex. The angle of refraction (θ_2) is determined from the dielectric constants and conductivities of the two media [Rei79]. The $\hat{n}_2\cos\hat{\theta}_2$ is complex and can be expressed as

$$\hat{n}_2\cos\hat{\theta}_2 = p + jq \tag{6.24}$$

$$p = \left[\frac{1}{2}\left\{(\varepsilon_{2r} - \varepsilon_1\sin\theta_1^2) + \sqrt{(\varepsilon_{2r} - \varepsilon_1\sin\theta_1^2)^2 + \varepsilon_{2i}^2}\right\}\right]^{\frac{1}{2}} \tag{6.25}$$

$$q = \left[\frac{1}{2}\left\{-(\varepsilon_{2r} - \varepsilon_1\sin\theta_1^2) + \sqrt{(\varepsilon_{2r} - \varepsilon_1\sin\theta_1^2)^2 + \varepsilon_{2i}^2}\right\}\right]^{\frac{1}{2}} \tag{6.26}$$

where $\varepsilon_{2r}=\varepsilon_2$ and $\varepsilon_{2i}=\sigma/\omega\varepsilon_0$. The dielectric constants of oxide and silicon are ε_1 and ε_2, respectively. The equation (6.26) can be derived using Snell's law. The transmission coefficients shown in (6.21) and (6.22) are complex which means they have an amplitude and a phase. Therefore, when wave travels through

the interface, the transmission coefficient attenuates the wave and adds a phase to the wave.

The second attenuation comes from the conductive silicon substrate. When the wave travels in silicon, it will be attenuated. The attenuation coefficient is [Wan86]

$$\alpha_{si} = \omega\sqrt{\frac{\mu\varepsilon}{2}}\left(\sqrt{1+\left(\frac{\sigma}{\omega\varepsilon}\right)^2}-1\right)^{\frac{1}{2}} \tag{6.27}$$

where σ is the conductivity, ω is the angular frequency, and the ε is the permittivity. The total attenuation through the silicon substrate is

$$A_{si} = \exp\left(-\alpha_{si}\frac{2d}{\cos\theta_2}\right) \tag{6.28}$$

where d is the thickness of the silicon substrate and θ_2 is the incident angle into the silicon substrate.

The third attenuation is from the attenuation factor (A) of the surface wave which travels at the bottom of the wafer as in path A. The total travel length (R) for the surface is

$$R = l - 2d\tan\theta_2, \tag{6.29}$$

where l is the distance between the receiving and the transmitting antennas. In this equation, the distance the wave travels in the oxide layer is ignored because the thickness of oxide is negligible. The attenuation factor A is

$$A = \exp[-\alpha_{sub}(l - 2d\tan\theta_2)] \tag{6.30}$$

α_{sub} is the attenuation coefficient of the surface wave.

If all the attenuation factors and phases are combined, the electric field traveling through path C is expressed as

$$\overline{E_C} = \frac{\overline{E}}{\hat{K}} t_{12} t_{21} \exp\left[(-\alpha_{si} - j\beta_{si})\frac{2d}{\cos\theta_2}\right] \exp[(-\alpha_{sub} - j\beta_{sub})(l - 2d\tan\theta_2)] \quad (6.31)$$

β_{si} is the propagation constant in silicon substrate and defined as

$$\beta_{si} = \omega\sqrt{\frac{\mu\varepsilon}{2}}\left(\sqrt{1+\left(\frac{\sigma}{\omega\varepsilon}\right)^2}+1\right)^{\frac{1}{2}} \quad (6.32)$$

β_{sub} is the propagation constant for the surface wave. In equation (6.31), the phase delay through the oxide layer is ignored because the thickness is negligibly thin compared to the thickness of the silicon.

Path D represents the wave traveling through the glass or air under the silicon substrate. There can be also multiple subpaths as shown in Figure 6-9. The wave traveling in this path suffers once again from three types of attenuation mechanisms. The first comes from transmission coefficients t_{12}, t_{21}, t_{23}, and t_{32}. The expression for the power transmission coefficient is given in (6.23).

The second is from the reflection coefficient between the silicon and glass or air. The expression for the power reflection coefficient is

$$R_{32} = \left(\frac{n_3\cos\theta_3 - \hat{n}_2\cos\hat{\theta}_2}{n_3\cos\theta_3 + \hat{n}_2\cos\hat{\theta}_2}\right)^2 \quad (6.33)$$

This is also complex because the silicon substrate is conductive. As the incident angle (θ_2) becomes smaller, the wave must be reflected a larger number

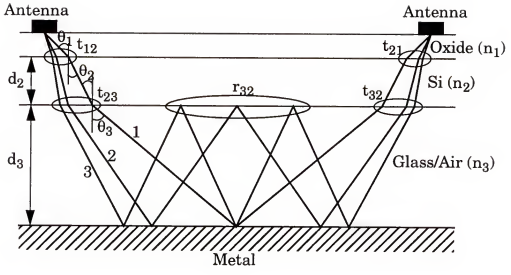


Figure 6-9 Possible ways of wave propagation in path D.

of times to reach the receiving antenna. As the number of reflections increase, the wave suffers more attenuation because the magnitude of R_{32} is less than 1. The reflection coefficient of the interface between the metal, and glass or air is close to -1. Therefore, there should be negligible loss when the wave is reflected on the metal surface.

The third attenuation mechanism is the conduction loss associated with the silicon substrate. The attenuation coefficient in silicon is given in (6.27).

The electric field component of the wave traveling through path D is

$$\overline{E_D} = \frac{\overline{E}}{R} t_{12} t_{21} t_{23} t_{32} \exp\left[(-\alpha_{si} - j\beta_{si})\frac{2d_2}{\cos\theta_2}\right]\exp\left[-j\beta_3\frac{2d_3}{\cos\theta_3} - j\pi\right] \quad (6.34)$$
$$+ \frac{\overline{E}}{R} t_{12}' t_{21}' t_{23}' t_{32}' r_{32}' \exp\left[(-\alpha_{si} - j\beta_{si})\frac{2d_2}{\cos\theta_2'}\right]\exp\left[-j\beta_3\frac{4d_3}{\cos\theta_3'}\right] + \ldots$$

In this equation, once again, the phase delay due to the oxide layer is ignored.

6.3.2 Experimental Results

The possible wave propagation paths were described in the previous section. The analyses of the attenuation and phase delays were based on the plane wave assumption. Even with the plane wave assumption, quantitative analyses of the wave propagation in each path is complicated. The electromagnetic field analysis of the actual antenna will be even more complicated because the actual electromagnetic wave from the antenna is not a plane wave. The difficulty of the analysis of the on-chip antenna arises from the complexity of the medium through which waves propagate. For the on-chip antenna transmission, five electrically different media are involved (air, oxide, silicon, metal, air/glass). This makes the theoretical analysis difficult. However, qualitative explanations of the experimental results are possible based on the discussion presented in the previous section and, in some cases, quantitative analyses and explanations of the measured results may also be possible. This section presents the experimental results of on-chip antennas in the measurement situation shown in Figure 6-5, and quantitative and qualitative explanations of the measured results.

Figure 6-10 shows transmission gain measurements of 2-mm zigzag dipole antennas on a 10 Ω–cm substrate. The oxide thickness is 3 μm. The distance between the receiving and the transmitting antennas is 5 mm. The wafer was put on 4-mm, 5-mm, and 6-mm thick glass layers on a metal chuck. The plots show dips at 11 GHz, 13 GHz, and 15.5 GHz for the measurements on 4-mm, 5-mm, and 6-mm thick glass slides, respectively. The measurements show that the change of the glass slide thickness changes the frequency at which the dip occurs. Since the change of the glass slide thick-

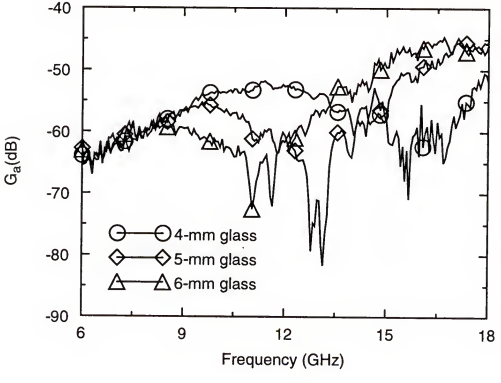


Figure 6-10 Transmission gain measurements of zigzag dipole antennas on a 10Ω-cm substrate on 4, 5, 6 mm thick glass slides.

ness only affects the waves traveling through path D, this implies that path D is a significant wave transmission path.

The dips are due to the interference between two or more electromagnetic waves with different phase velocities and transmission paths. When the phase difference between the two electromagnetic waves is 180^0 and the amplitudes are comparable, the two waves will destructively interfere each other (this shows up as a dip in the gain plot). From the frequencies at which the dips occur and the glass slide thicknesses, it is possible to compute the wavelength inside the glass slides. The dips in the transmission gain plot can be explained if we assume that the path A and path D are the dominant wave transmission paths, as shown in Figure 6-11.

The dielectric constants of air and silicon are known. However, that of the glass slide is not precisely known. To compute the phase delay of the waves in path D, the dielectric constant of glass should be known. However, if the length of the wave propagation paths are known, then the dielectric constant of the glass can be calculated from the frequencies at which the dips occur.This estimation involves an iteration technique. In the first iteration, since the thicknesses of the oxide (d1= ~3μm) and silicon substrate (d_2=0.5mm) are much smaller than that of the glass (d_3=4~6 mm), θ_1, θ_2, and θ_3 can be assumed to be the same and the lengths of the wave paths l_2 and l_3 can be estimated without much error. In this calculation, the phase delay through the oxide layer is ignored because the oxide layer is negligibly thin.

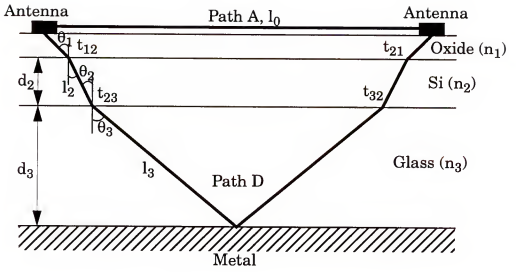


Figure 6-11 Wave propagation paths for a pair of on-chip antennas.

It is assumed that the power reflection coefficient of the interface between the glass and the silicon is very small so that the multiply reflected waves can be ignored. Let $\theta_2 = \theta_3 = \theta$, then

$$l_0 \cong 2(d_2 + d_3)\tan\theta \ . \tag{6.35}$$

Since l_0, d_2, and d_3 are known, θ can be calculated using (6.35). Once θ is known, l_2 and l_3 are calculated from

$$l_2 = \frac{d_2}{\cos\theta}, \tag{6.36}$$

$$l_3 = \frac{d_3}{\cos\theta}. \tag{6.37}$$

In order to maximize the destructive interference, the phase difference between path A and D should be π. Since the reflection at the metal plate in

path D will add π to the phase, the difference in phase should be 2π. The following equation should be satisfied to maximize the destructive interference.

$$k_3 2l_3 + k_2 2l_2 + phase(t_{12}t_{23}t_{32}t_{21}) - k_0 l_0 = 2\pi \tag{6.38}$$

where k_0, k_2, and k_3 are the wave numbers in air, silicon, and glass, respectively. If we assume that the phase delays associated with the transmission coefficients can be ignored, then (6.38) becomes

$$\frac{2l_1}{\lambda_1} + \frac{2l_2}{\lambda_2} - \frac{l_0}{\lambda_0} = 1 \tag{6.39}$$

Since l_0, l_1, and l_2 are known and λ_1 and λ_0 can be calculated from the frequencies of the dips, λ_2 can be calculated from (6.39). The dielectric constant of the glass can be calculated from

$$\varepsilon_r = \left(\frac{\lambda_0}{\lambda_2}\right)^2. \tag{6.40}$$

The calculation result using the measurements shown in Figure 6-10 reveals that the dielectric constant of the glass is ~4.8. This dielectric constant was calculated assuming that the phase delays associated with the transmission coefficients are negligible. In fact, the phase delays of the transmission coefficients can not be ignored.

From the computed dielectric constant of 4.8 and Snell's law, the estimations of θ_1, θ_2, and θ_3 can be improved using the following equations.

$$l_0 \cong 2(d_3 \tan\theta_3 + d_2 \tan\theta_2) \tag{6.41}$$

$$n_1 \sin\theta_1 = n_2 \sin\theta_2 = n_3 \sin\theta_3 \tag{6.42}$$

Equation (6.42) represents Snell's law. The transmission coefficients can be calculated using (6.21) and (6.22). The computed incident angles and phases of transmission coefficients are shown in Table 6-1. The re-calculated dielectric constant using the phase delays is ~4.3. Another iteration of the computation of the dielectric constant using the above value (4.3) also gives ~4.3, suggesting convergence. Since the dielectric constant has been determined, the total phase of the wave traveling through path D can be computed. The magnitudes of the power transmission coefficients are ~0.9 and the total power loss due to the transmission coefficients is ~-2.2 dB for all three glass thicknesses. The transmission coefficient of ~0.9 implies that the magnitude of the reflection coefficient is ~0.1. Therefore, the power of the multiply

Table 6-1 Incident angles and phases of transmission coefficients

Thickness of Glass	4 mm	5 mm	6 mm
Frequency of dip	15.5 GHz	13 GHz	11 GHz
θ_2	18.61°	15.69°	13.51°
Phase (t_{12})	7.7°	7.87°	8°
Phase (t_{23})	-20.75°	-20.34°	-19.97°
Phase (t_{32})	8.52°	8.56°	8.63°
Phase (t_{21})	-20.16°	-19.65°	-19.32°
Total phase	-24.69°	-23.56°	-22.66°

reflected wave in path D is less than 10% of that of the main wave shown in Figure 6-11 and neglecting the multiple reflections is justified.

As stated in section 6.3.1, the wave travels through path D suffers attenuation also due to the conductive silicon substrate. This attenuation depends on the length l_2. The attenuation coefficient is given in (6.27). The attenuation through the silicon substrate (G_s) is

$$G_s = 20\log(e^{-2\alpha_{si}l_2}) \tag{6.43}$$

The G_s is ~-4.4 dB for all three glass thicknesses. The total loss through path D is ~-6.6 dB. Since the wave traveling through path A is attenuated by ~-7 dB due to the surface wave attenuation factor, the two wave should have comparable amplitudes. However, the power of the wave in path D is about 7~8 dB (50 to 60% in amplitude) less than that of the wave in path A due to 1/R dependence of the field from the antenna. The R is the total distance the wave travels. The total distance in path D is about 2 to 3 time longer than that in path A depending on the thickness of the glass layer.

Figure 6-12 shows simulation and measurement results of transmission gains of antennas on glasses. The simulations were done assuming two plane waves. The sum of the two plane waves can be expressed as follows

$$E = A\exp(-jk_0l_0) + B\exp[-j2(k_3l_3 + k_2l_2) + Phase(t_{12}t_{23}t_{32}t_{21}) - j\pi] \tag{6.44}$$

A and B are the amplitudes of the waves and B is assumed to be 50 to 60% smaller than A. The plots show that the measured and simulated dip locations are matched. The simulated transmission gain curves show broader

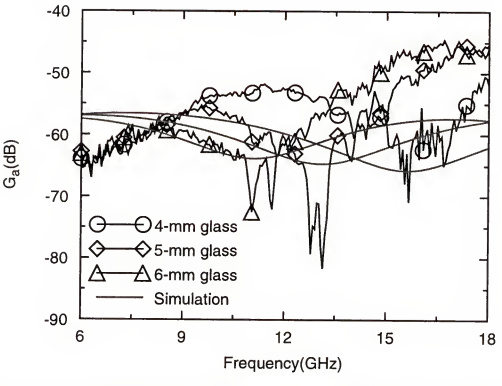


Figure 6-12 Transmission gain measurements of zigzag dipole antennas on 10Ω-cm substrate on 4, 5, 6 mm thick glass slides and simulation results using plane wave assumption.

and shallower dips because the amplitudes of the waves in path A is much larger than that of path D. In the calculation of the amplitudes of the waves, changes in the power efficiency due to changes in the wavelengths were not taken into account. Since the power efficiency of a dipole antenna depends on the antenna length in terms of the wavelength and the wavelength of the wave in path D should be much shorter (2 ~ 3 times) than that in the air, the power efficiency of the antenna for the waves in path D should be higher than that for the waves in path A. If the power efficiency is taken into account for the calculation of the power transmission gain, then the power level of the

wave in path D should be closer to that in path A. In that case, the dips should be deeper and sharper than those shown in the Figure 6-12.

Since this simulation did not include the frequency dependence of amplitudes for the plane waves, the gain values are not matched. However, it shows that the dips in the transmission gain plots can be explained by the addition of two plane waves. This result indicates that the electromagnetic waves from on-chip antennas travel through more than one path.

The phases of the sums of two plane waves are computed using (6.44) and shown in Figure 6-13. The plots show simulated phases of the antennas

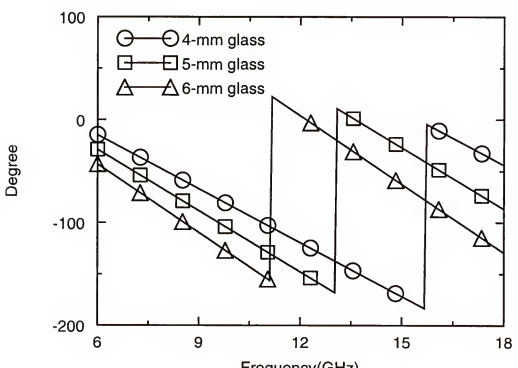


Figure 6-13 Phases of sums of two waves computed from simulation results.

on 4-mm, 5-mm, and 6-mm thick glass layers. The plot shows that the slopes of the phase plots are slightly different from each other. The phase velocities of the waves can be computed from the slopes of the phases. The computation results show that the phase velocities are 10.28×10^9 cm/sec, 9.08×10^9 cm/sec, and 8.11×10^9 cm/sec for 4-mm, 5-mm, and 6-mm cases, respectively. When the thickness of the glass is increased, the length of the propagation path of the waves in path D is increased. The increase of the length is translated to the slower phase velocity for the wave.

Figure 6-14 shows transmission gain measurements of zigzag dipole antennas on an air gap on a metal plate. Unlike the glass slide case, the

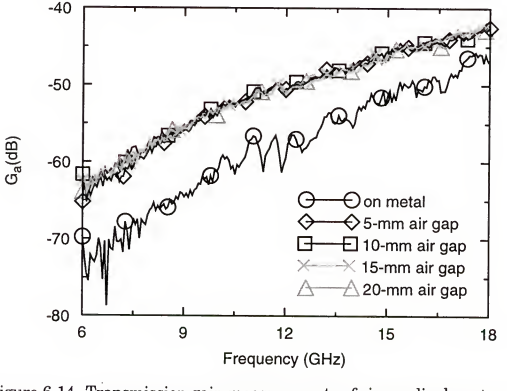


Figure 6-14 Transmission gain measurements of zigzag dipole antennas on 10Ω-cm substrate on air gap and on metal.

change of the thickness of the air gap does not change the gain. This implies that for this case, the wave traveling through path D is not significant. The possible reason is the fact that the wavelength in path D is comparable to that in the air. Therefore, the benefit of the reduced wavelength (increased power efficiency) is not present in this case while it suffers greater loss due to the 1/R dependence since the length of the path is longer than that of the other paths (paths A, B, C). On the other hand, the plot shows that the transmission gain of the antennas on a metal plate is 5 to 10 dB less than those on the air gaps. When the on-chip antennas are placed on a metal plate, the wave propagation through paths C and D are eliminated and the wave can only propagate through path A. This indicates that the wave propagation through path A is not dominant either. Therefore, the measurement results shown in Figure 6-14 suggests that path C is the dominant wave propagation path. It is speculated that the reason for the dominance of path C is due to the fact that the critical angle is fairly small (17^{o}). Further investigations will be necessary to verify the wave propagation path for the air gap case.

6.4 Summary

The electromagnetic field analysis of an Hertzian dipole antenna in a three layered medium was introduced. The three layered medium consists of air, a thin dielectric, and a conductor. The antenna was assumed to be on the interface between air and the dielectric. The electromagnetic field components were given and phase delays of the electric field component were com-

puted. Phase velocities were computed from the phase delay plot. The phase velocity of the wave traveling along the surface of the dielectric is bounded by the phase velocity in air on the high end and by that in the dielectric in the lower end. Especially, when the thickness of the dielectric is much smaller than a wavelength, phase velocity is close to that in air. A measurement result using on-chip antennas on metal plate verified the result from the analysis.

Possible paths for wave propagation have been investigated. There are three main paths for on-chip antenna electromagnetic wave transmission. The first is the direct wave transmission path between the transmitting and the receiving antennas. The second is the path through the silicon substrate and reflecting at the back surface of the silicon wafer. The third is the path through the silicon substrate and the glass or air under the silicon substrate. The phase and loss of the waves traveling through each path were computed.

Measurements of on-chip antennas on a glass layer showed dips in the transmission gain versus frequency measurements. The dips in the transmission gain measurements were explained by interference of two waves with different phase velocities. The dielectric constant of the glass was estimated from the frequencies at which dips occur and thicknesses of silicon and glass. The computation showed that it is ~4.3. These demonstrated that there can be a multiple number of wave propagation paths for electromagnetic wave transmission from on-chip antennas.

On-chip antennas on an air gap were also measured. Unlike the glass case, this measurement did not show any dips and a change of the air gap height did not change the gain. This result suggests that the power transmission through the air gap is not significant. Further investigations will be necessary to positively identify the wave propagation paths for the air gap case.

CHAPTER 7
SUMMARY AND SUGGESTIONS FOR FUTURE WORK

7.1 Summary

A Wireless clock distribution system has been proposed as an alternative approach for clock distribution. The system requires high frequency (~20 GHz) RF components implemented using a standard CMOS process. The feasibility of implementing the components including on-chip inductors, tuned amplifiers, and integrated antennas using standard CMOS processes was investigated.

A biased n-well inductor was proposed to reduce parasitic capacitance and to improve Q. This inductor does not require any non-standard practices. The inductor consists of a metal spiral, a poly resistor, and an n-well. The n-well is placed under the metal spiral and biased through the poly resistor. The poly resistor isolates the n-well from ac ground. The measurement results shows that 3-V reverse bias to the n-well reduces the parasitic capacitance by a factor of 2 and increases Q by 10%. The biased n-well inductor was fabricated using a p^- on p^+ wafer. The increase of the depletion region is limited by the p^+ layer. Use of p^- wafers should further decrease the parasitic capacitance or increase Q. 0.6-nH inductors for a 13-GHz tuned amplifier were fabricated on SOS and SOI substrates. Even at frequencies greater than

10 GHz, the measured inductance is close to the designed value predicted by Grover's method. Q factors of the inductors are 8 and 6.5 at 12.5 GHz, for the inductors on the SOS and SOI substrates, respectively. The Q factors of both inductors increase monotonically in the measurement frequency range between 11 and 15 GHz, which implies that the Q can be improved by optimizing the inductor design to have the peak Q at the operating frequency. This also implies that inductor design for higher frequency operation (~20 GHz) with even higher Q is possible.

Design and measurement results of a 13-GHz tuned amplifier were presented. The amplifier is the first in a CMOS technology to have a tuned frequency greater than 10 GHz. Partially scaled 0.1-μm CMOS process was used for fabrication. The amplifier was implemented on SOS and SOI substrates. The amplifier uses a 3-stage design. The first two stages are cascodes with an inductive load, and the last stage is a common source with a resistive load. All the circuit gain is generated by the first two stages and the last stage is for driving a 50-Ω load. Input and output matching networks are not included on-chip. The measurement results show that the transducer gains are 15 dB and 5.3 dB for the SOS and SOI amplifiers, respectively. The 50-Ω noise figures are 7 dB and 9.1 dB for the SOS and SOI amplifiers. The reverse isolation for both amplifiers are similar and greater than 37 dB. The power consumptions are 45 mW and 58 mW for the SOI and SOS amplifiers on a power supply of 1.5V. The low gain and resonance frequency of the SOI amplifier is mainly due to the back-gate parasitic capacitances. The measure-

ment results of the amplifiers suggest that ~20 GHz amplifier may be possible using CMOS technologies.

Antenna test structures and an antenna measurement set-up were described. Antenna test structures were fabricated using an IBM CMOS process and the UF process. The UF process was developed for antenna test structure fabrication in a large chip (~5x4 cm^2). The UF process has one metal layer with no passivation. An antenna measurement set-up has been developed for on-chip antenna characterization. The measurement set-up uses a vector network analyzer, baluns, signal-signal probes, and a probe station. Phase and gain mismatches of baluns and semi-rigid cables were measured. It was shown that the mismatches of the baluns can be reduced by properly selecting semi-rigid cables. The phase delay and loss measurements of cables using a balanced and an unbalanced measurement set-up were presented. It has been shown that the phase and gain measurements of semi-rigid cables using the balanced and the unbalanced measurement set-up are equivalent.

The feasibility of implementing integrated antennas for a wireless clock distribution system was also investigated. Linear, meander, zigzag dipole, and loop antennas were fabricated and characterized. An increase of length and width, and a decrease of bend angle increase the transmission gains for dipole antennas. For loop antennas, increasing metal width increases the transmission gain. The transmission gain is decreased by 10dB/ doubling of the distance between the receiving and transmitting antennas.

The conductivity of the substrate affects the gain of integrated antennas. Antennas on SOS shows ~25 dB higher gains than those on a 20 Ω–cm silicon substrate. The oxide thickness does not affect the gain much for antennas fabricated on the 20 Ω-cm substrate. Radiation pattern measurements of the linear, meander, and zigzag dipole antennas showed that the patterns are similar to that of a normal small dipole antenna. The measured radiation pattern of the loop antenna is isotropic. The transmission gain measurement of antennas on the SOS substrate, the frequency dependence of the phase, and radiation pattern measurements strongly indicate that the signal transmission between receiving and transmitting antennas occurs through electromagnetic wave propagation rather than through the RC coupling. A 2-mm long, 30-μm wide, 30-degree zigzag dipole antenna pair on a 20-Ω–cm substrate shows -45 dB gain for a separation of 1 cm and -56 dB for 2-cm separation near 18 GHz. A loop-zigzag dipole pair shows ~4 dB less gains than the zigzag dipole pair. The loop diameter is 200 μm and the metal width is 10 μm. It has been shown that a 7.4 GHz clock receiver in a 0.25-μm CMOS technology can lock to a -43 dBm input signal [Flo00]. Since the loop-zigzag dipole pair shows gains greater than -60 dB for separation of 2 cm near 18 GHz, if the antennas, receiver and transmitter are matched, then a clock receiver with a zigzag dipole antenna 2 cm away from a transmitter using a loop antenna should be able lock to a 20-dBm clock signal delivered to the transmitting antenna. If the operating frequency is increased, the required transmission power is expected to be lowered. The loop antenna with a compact

size and an isotropic radiation pattern is ideal as the transmitter antenna for a wireless clock distribution system. This work showed that wireless interconnection in an area of 2-cm radius is possible in the absence of interference structures using integrated antennas.

Lastly, the electromagnetic wave propagation from on-chip antennas was investigated. A theoretical analysis of electromagnetic fields generated by an Hertzian dipole antenna in a three layered medium was introduced. The three layered medium consists of air, a thin dielectric, and a conductor. The air and conductor are assumed to be semi-infinite. The analysis and measurements showed that the phase velocity of waves traveling on dielectric surface is that in air when the thickness of the dielectric is much smaller than the wavelength. Possible paths for wave propagation from on-chip antennas were investigated. It is shown that there are three main paths for electromagnetic wave transmission from on-chip antennas. Phase delay and loss associated with each wave propagation path were investigated. The power transmission gain versus frequency measurements of on-chip antennas on glass layer showed dips. The dips were explained by interference between two waves with different phase velocities and path lengths. The dielectric constant of the glass was calculated from the frequencies where the dips occur and thicknesses of the glass and silicon substrate. On-chip antennas on an air gap were also measured. The measurement results showed that the transmission gain is not affected by the height of the air gap. This result suggests that the power transmission through the air gap is not significant.

This investigation showed that there are multiple wave propagation paths in electromagnetic wave transmission between two on-chip antennas.

The antenna work presented in this dissertation is new in antenna research. Previous work on integration of antennas in ICs has used ceramic and GaAs substrates. This work has shown that the integration of antennas in silicon ICs is possible and the wireless communication using such antennas is feasible for the first time.

7.2 Suggestions for Future Work

To implement a wireless clock distribution system, the clock receiver should not use any external components. Therefore, design of high Q on-chip inductors are necessary. In Chapter 2, it is shown that 0.6-nH inductors on SOS and SOI substrates have Q factors of 8 and 6.5 at 12.5 GHz. The process used for the fabrication of the 0.6 nH inductor has only two metal layers. Deep sub-micron CMOS processes are expected to have 6~7 levels of metal (Copper) and low k dielectric layers. Using such processes, design of high Q (~40) inductor with low parasitics for high frequency application should be achievable.

The 13 GHz tuned amplifier implemented in this work has shown that an amplifier with an operating frequency greater than 10 GHz using a CMOS technology is possible. However, the noise, matching, and linearity performances of the amplifier were not acceptable. These need to be improved. Using a CMOS process with Copper and multiple (6~7) metal layers, it

should be possible to integrate the matching networks. The performances of the amplifier should get much better by integrating the matching networks and optimizing the design.

The antenna measurement set-up used in this work can only be used for on-chip antennas. In order to investigate inter-chip wireless clock distribution systems using external antennas, it is necessary to develop a new measurement set-up which can measure S-parameters between an on-chip antenna and an external antenna.

Antenna fabrication process needs to be improved. The process developed in this work supports only one metal layer. To emulate real IC environments and investigate interference from metal structures above, below, and between receiving and transmitting antennas, at least three metal layers are necessary. The three level metal process can also be used to investigate the shielding effects of metal structures surrounding antennas.

The losses and phase delays of wave propagation were studied based on the plane wave assumption. It was assumed that waves propagating each direction from the antenna have the same amplitudes. Using this analysis, the dips in the transmission gain measurements of on-chip antennas on glass slides were successfully explained. However, this model can not be used to predict all the antenna performance. In order to fully explain the behaviors of on-chip antennas, a full wave 3-D EM simulation capability will be necessary. A complete analytical description of on-chip antennas will be prohibitively complex. Simulation capabilities should provide much more freedom to inves-

tigate various antenna structures, substrate effects, interferences, and so forth.

The measurements of on-chip antennas on air did not show any dips in the gain plots. It was speculated that this is because one path is dominant. However, this assertion was not quantitatively supported. A quantitative analysis of this problem is necessary to understand the wave propagating mechanism in the air-gap case.

APPENDIX A
ANTENNA FABRICATION PROCEDURE

This fabrication procedure for integrated antennas in Microelectronics Lab. in the University of Florida is described.

Before the fabrication, wafers are cleaned using Acetone, Methanol, and DI water, and dried.

1 . Oxidation using a furnace.

Instructions for using diffusion furnaces are in the Lab and the oxidation time and temperatures can be obtained from reference [Jae93]. The temperature of the furnaces can be set using switches on the front panel of the furnaces. Refer to the instructions.

(1) Turn on the furnace according to the instruction. It takes about 30 minutes to turn it on.

(2) To use wet O_2, make sure the bubbler on the back of the furnace is filled. Since the bubbler is not refilled automatically, it is necessary to check and refill the bubbler manually during the oxidation.

(3) Push wafers into the furnace. It is required to stop for 30 second between each push. Place the wafers in the center of furnace with 3 pushes.

(4) Close the furnace and wait until the required oxidation time is elapsed.

(5) Open the furnace and pull out the wafer. Pull out takes about 1 minute with 2 ~ 3 pull steps.

(6) Let the wafers cool down and measure the oxide thickness with Nanospec.

2 . Before Aluminum e-beam deposition, clean the wafers using Acetone, Methanol, and DI water, and dry the wafers. This step is not required, if Aluminum is deposited within the same day as the oxidation.

3 . Deposit Aluminum using an e-beam machine. The instructions are on the machine. A typical thickness ranges between 1 and 3 μm.

4 . Photolithography

(1) Prebake: 110°C 30 min in a hard bake oven.

(2) Put a wafer on the spinner, apply photo resist (AZ1529), and Spin the wafer: 3000 RPM, 50sec.

(3) Put the wafer into the oven for soft bake: 90°C, 30 min.

(4) Expose the wafer using the mask aligner: expose time 15 sec. The instruction for the mask aligner is on the machine. The expose time varies. Check with the previous user.

(5) Develop the wafer using MIF 312 diluted developer: Put the wafer in the developer for 1 to 2 min. Make sure all the photoresist is

removed in the exposed areas. After the development, wash the wafer in DI water and dry using a nitrogen gun.

(6) Put the wafer into the oven for hard bake: 110°C, 30 min.

5 . Inspect the wafers under a microscope to make sure that the photo lithography step is properly executed. If not remove the photoresist using Acetone and repeat step 4.

6 . Aluminum etch using aluminum etchant.

(1) Put the patterned wafer in the aluminum etchant for 3.5 min (for 2 μm thick aluminum).

(2) Wash the wafer with DI water and dry the wafer with a nitrogen gun.

(3) Inspect the wafer under a microscope to make sure that all the Aluminum is removed from the area not protected by the photoresist. If not, etch the wafer for 1 additional minute using steps 6 (1), and 6 (2).

(4) Remove the photoresist using Acetone.

(5) Clean the wafer using Methanol and DI water.

(6) Dry the wafer.

APPENDIX B
180 DEGREE HYBRID COUPLER

An 180° hybrid coupler is a four port network with a 180° phase shift between the two output ports [Poz82]. The coupler can also generate in phase outputs. Figure B-1 shows the symbol for a 180° hybrid coupler. When a signal is applied to port (1) (Σ port), the signal will be evenly split and signals with the same amplitude and phase will come out from port (3) and (4). Port (4) will be isolated. If a signal is applied to port (4) (Δ port), the signal will be evenly split with a 180° phase difference and 180° out of phase signals with the same amplitude will come out from ports (2) and (3). In this case, port (1) will be isolated. When it is used as a combiner with two input signals applied to ports (2) and (3), the sum will come out from port (1) and the difference will

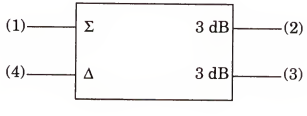


Figure B-1 Symbol for a 180° hybrid coupler.

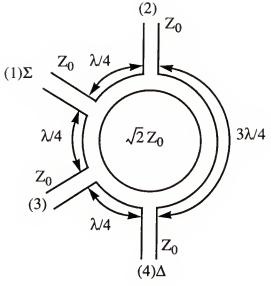


Figure B-2 A ring hybrid coupler in microstrip form.

come out from port (4). When a port is not used, it should be terminated with the characteristic impedance Z_0.

This Appendix presents an analysis of a ring hybrid with arbitrary but equal loads connected to ports (2) and (3). Typically, characteristics of hybrids are specified with loads of Z_0. Since for antenna measurements, the loads can significantly deviate from Z_0, the impact of this on the operation of hybrid should be analyzed. The band width of the ring hybrid is generally about 20 ~ 30% of the center frequency. This band width can be increased by using additional sections or a symmetric ring circuit. Figure B-2 shows a microstrip type ring hybrid coupler.

The ring hybrid coupler can be analyzed using a simplified circuit model shown in Figure B-3. The impedances are normalized with Z_0. At port (2) and (3), loads with arbitrary impedance is connected in series with Z_0. Z is the normalized impedance looking into one of the two feed lines for antennas transformed by a transmission line. First, let's compute S_{24}. There are two signal paths between port (4) and port (2). One path is through a $3\lambda/4$ transmission line and the other is through ports (3) and (1). Let's call the former path as path A and the latter as path B. Since the two paths are connected in parallel, if we compute Y-parameters of path A and paths B, the Y-parameters between ports (4) and (2) can be easily computed by adding them together. The Y-parameter of path A is

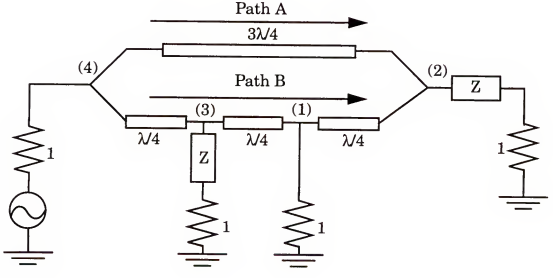


Figure B-3 A simplified circuit diagram of a ring hybrid coupler.

$$Y_A = \begin{bmatrix} 0 & \frac{-j}{\sqrt{2}} \\ \frac{-j}{\sqrt{2}} & 0 \end{bmatrix}. \tag{B.1}$$

Since the transmission lines and shunt impedances are in path B are cascaded, the Y-parameter can be computed easily using ABCD parameters of subsections. The ABCD parameters of path B is

$$\begin{bmatrix} a & b \\ c & d \end{bmatrix} = \begin{bmatrix} 0 & j\sqrt{2} \\ \frac{j}{\sqrt{2}} & 0 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ \frac{1}{Z+1} & 1 \end{bmatrix}\begin{bmatrix} 0 & j\sqrt{2} \\ \frac{j}{\sqrt{2}} & 0 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}\begin{bmatrix} 0 & j\sqrt{2} \\ \frac{j}{\sqrt{2}} & 0 \end{bmatrix} = \begin{bmatrix} \frac{-j\sqrt{2}}{Z+1} & \frac{-j\sqrt{2}(Z+3)}{Z+1} \\ \frac{-j}{\sqrt{2}} & -j\sqrt{2} \end{bmatrix}. \tag{B.2}$$

The ABCD parameters can be easily converted into Y-parameters.

$$Y_B = \begin{bmatrix} \frac{Z+1}{Z+3} & \frac{-j}{\sqrt{2}}\left(\frac{Z+1}{Z+3}\right) \\ \frac{-j}{\sqrt{2}}\left(\frac{Z+1}{Z+3}\right) & \frac{1}{Z+3} \end{bmatrix} \tag{B.3}$$

The Y-parameters between ports (4) and (2) is

$$Y = Y_A + Y_B = \left(\frac{1}{Z+3}\right)\begin{bmatrix} Z+1 & -j\sqrt{2}(Z+2) \\ -j\sqrt{2}(Z+2) & 1 \end{bmatrix} \tag{B.4}$$

Since the arbitrary impedance Z at port (2) is connected in series with the termination impedance, it is necessary to convert equation (B.4) to ABCD parameters and multiply them by the ABCD parameters of Z.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \frac{-j}{\sqrt{2}}\left(\frac{1}{Z+2}\right)\begin{bmatrix} 1 & Z+3 \\ 2Z+3 & Z+1 \end{bmatrix}\begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} = \frac{-j}{\sqrt{2}}\left(\frac{1}{Z+2}\right)\begin{bmatrix} 1 & 2Z+3 \\ 2Z+3 & 2Z^2+4Z+1 \end{bmatrix} \tag{B.5}$$

S_{24} can be computed from equation (B.5).

$$S_{24} = \frac{2}{A+B+C+D} = j\sqrt{2}\left(\frac{1}{Z+2}\right) \tag{B.6}$$

S_{34} can also be computed using the same technique used to compute S_{24}. In this case, path A is the transmission line with a length of $\lambda/4$ and path B is the path through ports (2) and (1). The Y-parameters of path A is

$$Y_A = \begin{bmatrix} 0 & \frac{j}{\sqrt{2}} \\ \frac{j}{\sqrt{2}} & 0 \end{bmatrix}. \tag{B.7}$$

The ABCD parameters of path B is

$$\begin{bmatrix} a & b \\ c & d \end{bmatrix} = \begin{bmatrix} 0 & -j\sqrt{2} \\ -\frac{j}{\sqrt{2}} & 0 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ \frac{1}{Z+1} & 1 \end{bmatrix}\begin{bmatrix} 0 & j\sqrt{2} \\ \frac{j}{\sqrt{2}} & 0 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}\begin{bmatrix} 0 & j\sqrt{2} \\ \frac{j}{\sqrt{2}} & 0 \end{bmatrix} = \begin{bmatrix} \frac{j\sqrt{2}}{Z+1} & \frac{j\sqrt{2}(Z+3)}{Z+1} \\ \frac{j}{\sqrt{2}} & j\sqrt{2} \end{bmatrix} \tag{B.8}$$

Once again, the ABCD parameters are converted to Y-parameters.

$$Y_B = \begin{bmatrix} \frac{Z+1}{Z+3} & \frac{j}{\sqrt{2}}\left(\frac{Z+1}{Z+3}\right) \\ \frac{j}{\sqrt{2}}\left(\frac{Z+1}{Z+3}\right) & \frac{1}{Z+3} \end{bmatrix}. \tag{B.9}$$

From Eq. (B.7) and Eq. (B.9),

$$Y = Y_A + Y_B = \left(\frac{1}{Z+3}\right)\begin{bmatrix} Z+1 & j\sqrt{2}(Z+2) \\ j\sqrt{2}(Z+2) & 1 \end{bmatrix} \tag{B.10}$$

These Y-parameters are converted to ABCD parameters and multiplied to the ABCD parameters of the series Z to obtain the ABCD parameters for the entire network.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \frac{j}{\sqrt{2}}\left(\frac{1}{Z+2}\right)\begin{bmatrix} 1 & Z+3 \\ 2Z+3 & Z+1 \end{bmatrix}\begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} = \frac{j}{\sqrt{2}}\left(\frac{1}{Z+2}\right)\begin{bmatrix} 1 & 2Z+3 \\ 2Z+3 & 2Z^2+4Z+1 \end{bmatrix} \quad \text{(B.11)}$$

Like S_{24}, S_{34} can be obtained using equation (B.11).

$$S_{34} = \frac{2}{A+B+C+D} = -j\sqrt{2}\left(\frac{1}{Z+2}\right) \quad \text{(B.12)}$$

(B.6) and (B.12) show that the input power is evenly divided into ports (2) and (3) with a 180^0 phase difference when arbitrary but equal impedances are connected to the two output ports.

APPENDIX C
ELECTROMAGNETIC FIELD ANALYSIS OF A HERTZIAN DIPOLE ANTENNA ON A SILICON SUBSTRATE

The analysis of electromagnetic field generated by a Hertzian dipole in a three-layered region can be carried out by using Maxwell's equations [Kin91, Kin92a]. The schematic diagram of a Hertzian dipole in a three-layered medium is shown in Figure C-1. In the case studied in this work, region 0 is air, region 1 is oxide (dielectric), and region 2 is silicon (conductor). When the thickness of the dielectric layer is very small compared to wavelength ($l << \lambda$), the analysis is similar to the analysis of the electromagnetic field gen-

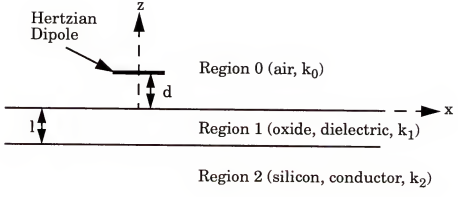


Figure C-1 A Hertzian dipole at height d over region 1 in a three-layered medium.

erated by a Hertzian dipole near the boundary between two different half spaces. The electromagnetic field of a Hertzian dipole in two different half spaces was first analyzed by Sommerfeld in 1909 [Som09]. He derived the general complex integrals for the vector potentials. The problem was studied to understand the electromagnetic wave propagation between two dipole antennas on the Earth. Norton and Baños obtained sets of simple approximated formulas from the Sommerfeld integrals [Nor36, Ban66]. Recently, explicit expressions for the integrals have been derived by King and were applied to three-layered medium problems [Kin91]. This appendix introduces the electromagnetic field analysis for a Hertzian dipole in a three-layered medium.

The analysis of the three layer problem can easily be accomplished using the analysis of the two layer problem. Therefore, we will start with the analysis of the electromagnetic field from a Hertzian dipole in two different half spaces, and then use the result to calculate the electromagnetic field from a Hertzian dipole in a three-layered medium. The geometry of the Hertzian dipole in two different half spaces is shown in Figure C-2. The Hertzian dipole is x-directed and located at z=d on z-axis. It is assumed that the two regions are non-magnetic so that $\mu_1=\mu_0$. The complex dielectric constants of the two regions are $\tilde{\varepsilon}_n=\varepsilon_n+i\sigma_n/\omega$, where n=0, 1. The wave numbers are $k_n=\beta_n+i\alpha_n=\omega\sqrt{\mu_0\tilde{\varepsilon}_n}$. Maxwell's equations in the two regions are

$$\nabla\times\bar{E}_n = i\omega\bar{B}_n \tag{C.1}$$

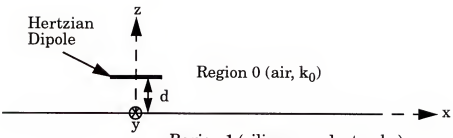


Figure C-2 A Hertzian dipole at height d over the interface between the two half spaces.

$$\nabla \times \vec{B}_n = \mu_0(-i\omega\tilde{\varepsilon}_n\vec{E}_n + \hat{x}J_x) \tag{C.2}$$

where

$$J_x = \delta(x)\delta(y)\delta(z-d)\,. \tag{C.3}$$

J_x is the volume density of current in the dipole normalized to have a unit electric moment (IΔl=1 A m). The boundary conditions to be satisfied by the solutions of the above Maxwell's equations are as follows.

On the boundary between region 0 and region 1,

$$E_{0x}(x, y, 0) = E_{1x}(x, y, 0)$$

$$E_{0y}(x, y, 0) = E_{1y}(x, y, 0)$$

$$k_0 E_{0z}(x, y, 0) = k_1 E_{1z}(x, y, 0) \tag{C.4}$$

$$\vec{B}_0(x, y, 0) = \vec{B}_1(x, y, 0) \tag{C.5}$$

Where k_0 and k_1 are the wave numbers in the region 0 and 1, respectively.

The translational invariance of the boundary in the x- and y-directions suggests the use of Fourier transform. Using Fourier transform, E and B can be expressed as follows,

$$\bar{E}(x, y, z) = \left(\frac{1}{2\pi}\right)^2 \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \bar{E}(\xi, \eta, z) e^{i(\xi x + \eta y)} d\eta d\xi \tag{C.6}$$

$$\bar{B}(x, y, z) = \left(\frac{1}{2\pi}\right)^2 \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \bar{B}(\xi, \eta, z) e^{i(\xi x + \eta y)} d\eta d\xi \tag{C.7}$$

The Fourier transform of $J_x(x,y,z)$ is

$$J_x(\xi, \eta, z) = \delta(z - d) \tag{C.8}$$

The transformed Maxwell's equations in Cartesian coordinates are

$$i\eta E_{nz} - \frac{\partial}{\partial z} E_{ny} = i\omega B_{nx} \tag{C.9}$$

$$\frac{\partial}{\partial z} E_{nx} - i\xi E_{nz} = i\omega B_{ny} \tag{C.10}$$

$$i\xi E_{ny} - i\eta E_{nx} = i\omega B_{nz} \tag{C.11}$$

$$i\eta B_{nz} - \frac{\partial}{\partial z} B_{ny} = -\frac{ik_n^2}{\omega} E_{nx} + \mu_0 \delta(z - d) \tag{C.12}$$

$$\frac{\partial}{\partial z} B_{nx} - i\xi B_{nz} = -\frac{ik_n^2}{\omega} E_{ny} \tag{C.13}$$

$$i\xi B_{ny} - i\eta B_{nx} = -\frac{ik_n^2}{\omega} E_{nz} \tag{C.14}$$

From the above equations, the following ordinary differential equations for E_{nx} and B_{nx} are obtained.

$$\left(\frac{d^2}{dz^2}+\gamma_n^2\right)E_{nx} = \frac{\omega\mu_0(k_n^2-\xi^2)}{ik_n^2}\delta(z-d) \tag{C.15}$$

$$\left(\frac{d^2}{dz^2}+\gamma_n^2\right)B_{nx} = 0 \tag{C.16}$$

where $\gamma_n^2 = k_n^2-\xi^2-\eta^2$.

The solutions for E_x and B_x in region 0 obtained from equations (C.15) and (C.16) using boundary conditions (C.4) and (C.5) are

$$B_{0x} = C_1 e^{i\gamma_0 z} \tag{C.17}$$

$$E_{0x} = C_2 e^{i\gamma_0 z} - \frac{\omega\mu_0(k_0^2-\xi^2)}{ik_0^2}e^{i\gamma_0 d}\sin\gamma_0 z;(0\le z\le d) \tag{C.18}$$

$$E_{0x} = \left(C_2 - \frac{\omega\mu_0(k_0^2-\xi^2)}{ik_0^2}\sin\gamma_0 d\right)e^{i\gamma_0 z};(d\le z) \tag{C.19}$$

$$C_1 = -\frac{\xi\eta(k_0^2-k_1^{\,2})}{MN}\mu_0 e^{i\gamma_0 d} \tag{C.20}$$

$$C_2 = -\frac{\gamma_0(k_1^2-\xi^2)+\gamma_1(k_0^2-\xi^2)}{MN}\omega\mu_0 e^{i\gamma_0 d} \tag{C.21}$$

where $M \equiv \gamma_1+\gamma_0$ and $N \equiv k_0^2\gamma_1+k_1^2\gamma_0$.

B_{0y}, B_{0z}, E_{0y}, and E_{0z} can be obtained using (C.9) - (C.14).

In region 0 with $d \le z$,

$$E_{0x} = -\frac{\omega\mu_0}{4\pi^2}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} e^{i(\xi x+\eta y)}\left(\frac{\gamma_0(k_1^2-\xi^2)+\gamma_1(k_0^2-\xi^2)}{MN}e^{i\gamma_0 d}+\frac{k_0^2-\xi^2}{i\gamma_0 k_0^2}\sin\gamma_0 d\right)e^{i\gamma_{0z}}d\xi d\eta \tag{C.22}$$

$$E_{0y} = \frac{\omega\mu_0}{4\pi^2}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} e^{i(\xi x+\eta y)}\left(\frac{\sin\gamma_0 d}{i\gamma_0 k_0^2}+\frac{e^{i\gamma_0 d}}{N}\right)e^{i\gamma_{0z}}d\xi d\eta \tag{C.23}$$

$$E_{0z} = \frac{\omega\mu_0}{4\pi^2}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} e^{i(\xi x+\eta y)}\left(\frac{\sin\gamma_0 d}{i\gamma_0 k_0^2}+\frac{\gamma_0 e^{i\gamma_0 d}}{N}\right)e^{i\gamma_{0z}}d\xi d\eta \tag{C.24}$$

$$B_{0x} = -\frac{\mu_0}{4\pi^2}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} e^{i(\xi x+\eta y)}\frac{k_0^2-k_1^2}{MN}e^{i\gamma_0(z+d)}d\xi d\eta \tag{C.25}$$

$$B_{0y} = \frac{\mu_0}{4\pi^2}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} e^{i(\xi x+\eta y)}\left(i\sin\gamma_0 d+\frac{k_1^2\eta^2-k_0^2(k_1^2-\xi^2+\gamma_0\gamma_1)}{MN}e^{i\gamma_0 d}\right)e^{i\gamma_{0z}}d\xi d\eta \tag{C.26}$$

$$B_{0z} = \frac{\mu_0}{4\pi^2}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} e^{i(\xi x+\eta y)}\left(\frac{\sin\gamma_0 d}{i\gamma_0}+\frac{e^{i\gamma_0 d}}{M}\right)e^{i\gamma_{0z}}d\xi d\eta \tag{C.27}$$

It is more convenient to use the cylindrical coordinate for evaluations of the above integrals. In order to change the Cartesian coordinate to the cylindrical coordinate, the following changes of variables are necessary.

$$x = \rho\cos\phi,\ y = \rho\sin\phi \tag{C.28}$$

The Cartesian transform variables also need to be changed to cylindrical transform variables.

$$\xi = \lambda\cos\phi',\ \eta = \lambda\sin\phi' \tag{C.29}$$

Then,

$$\gamma_n = \sqrt{k_n^2-\lambda^2},\ \text{n=0, 1} \tag{C.30}$$

$$\xi x + \eta y = \lambda\rho\cos(\phi - \phi'),\ d\xi d\eta = \lambda d\phi' d\lambda \tag{C.31}$$

The cylindrical components of the electric field are given by

$$E_\rho = E_x\cos\phi + E_y\sin\phi,\ E_\phi = -E_x\sin\phi + E_y\cos\phi \tag{C.32}$$

Using the cylindrical coordinate, the electromagnetic field components can be expressed as

$$E_{0\rho} = -\frac{\omega\mu_0}{4\pi k_0^2}\cos\phi\left[\int_0^\infty\left(k_0^2 J_0(\lambda\rho) - \frac{\lambda^2}{2}\{J_0(\lambda\rho) - J_2(\lambda\rho)\}\right)\gamma_0^{-1}e^{i\gamma_0|z-d|}\lambda d\lambda \right. \tag{C.33}$$
$$\left. + \int_0^\infty\left(\frac{\gamma_0 Q}{2}\{J_0(\lambda\rho) - J_2(\lambda\rho)\} - \frac{k_0^2 P}{2\gamma_0}\{J_0(\lambda\rho) + J_2(\lambda\rho)\}\right)e^{i\gamma_0(z+d)}\lambda d\lambda\right]$$

$$E_{0\phi} = \frac{\omega\mu_0}{4\pi k_0^2}\sin\phi\left[\int_0^\infty\left(k_0^2 J_0(\lambda\rho) - \frac{\lambda^2}{2}\{J_0(\lambda\rho) + J_2(\lambda\rho)\}\right)\gamma_0^{-1}e^{i\gamma_0|z-d|}\lambda d\lambda \right. \tag{C.34}$$
$$\left. + \int_0^\infty\left(\frac{\gamma_0 Q}{2}\{J_0(\lambda\rho) + J_2(\lambda\rho)\} - \frac{k_0^2 P}{2\gamma_0}\{J_0(\lambda\rho) - J_2(\lambda\rho)\}\right)e^{i\gamma_0(z+d)}\lambda d\lambda\right]$$

$$E_{0z} = \frac{i\omega\mu_0}{4\pi k_0^2}\cos\phi\int_0^\infty(e^{i\gamma_0|z-d|} - Qe^{i\gamma_0(z+d)})J_1(\lambda\rho)\lambda^2 d\lambda \tag{C.35}$$

$$B_{0\rho} = -\frac{\mu_0}{4\pi}\sin\phi\left[\int_0^\infty e^{i\gamma_0|z-d|}J_0(\lambda\rho)\lambda d\lambda + \right. \tag{C.36}$$
$$\left.\int_0^\infty\left(\frac{Q}{2}\{J_0(\lambda\rho) + J_2(\lambda\rho)\} - \frac{P}{2}\{J_0(\lambda\rho) - J_2(\lambda\rho)\}\right)e^{i\gamma_0(z+d)}\lambda d\lambda\right]$$

$$B_{0\phi} = -\frac{\mu_0}{4\pi}\cos\phi\left[\int_0^\infty e^{i\gamma_0|z-d|}J_0(\lambda\rho)\lambda d\lambda + \right. \tag{C.37}$$
$$\left.\int_0^\infty\left(\frac{Q}{2}\{J_0(\lambda\rho) - J_2(\lambda\rho)\} - \frac{P}{2}\{J_0(\lambda\rho) + J_2(\lambda\rho)\}\right)e^{i\gamma_0(z+d)}\lambda d\lambda\right]$$

$$B_{0z} = \frac{i\mu_0}{4\pi}\sin\phi\int_0^\infty(e^{i\gamma_0|z-d|} - Pe^{i\gamma_0(z+d)})\gamma_0^{-1}J_1(\lambda\rho)\lambda^2 d\lambda \tag{C.38}$$

where P and Q are

$$P \equiv \frac{\gamma_0 - \gamma_1}{\gamma_0 + \gamma_1} \tag{C.39}$$

$$Q \equiv \frac{k_1^2\gamma_0 - k_0^2\gamma_1}{k_1^2\gamma_0 + k_0^2\gamma_1} \tag{C.40}$$

If the above integrals are rearranged, the following equations are obtained.

$$E_{0\rho} = -\frac{\omega\mu_0}{4\pi k_0^2}\cos\phi[F_{\rho 0}(\rho, z-d) - F_{\rho 0}(\rho, z+d) + F_{\rho 1}(\rho, z+d)] \tag{C.41}$$

where

$$F_{\rho 0}(\rho, z-d) \tag{C.42}$$
$$= \int_0^\infty \left(\frac{\gamma_0}{2}\{J_0(\lambda\rho) - J_2(\lambda\rho)\} + \frac{k_0^2}{2\gamma_0}\{J_0(\lambda\rho) + J_2(\lambda\rho)\} \right) e^{i\gamma_0|z-d|}\lambda d\lambda$$

$$F_{\rho 0}(\rho, z+d) \tag{C.43}$$
$$= \int_0^\infty \left(\frac{\gamma_0}{2}\{J_0(\lambda\rho) - J_2(\lambda\rho)\} + \frac{k_0^2}{2\gamma_0}\{J_0(\lambda\rho) + J_2(\lambda\rho)\} \right) e^{i\gamma_0(z+d)}\lambda d\lambda$$

$$F_{\rho 1}(\rho, z+d) \tag{C.44}$$
$$= \int_0^\infty \left(\frac{\gamma_0}{2}(Q+1)\{J_0(\lambda\rho) - J_2(\lambda\rho)\} - \frac{k_0^2}{2\gamma_0}(P-1)\{J_0(\lambda\rho) + J_2(\lambda\rho)\} \right) e^{i\gamma_0(z+d)}\lambda d\lambda$$

$$E_{0\phi} = \frac{\omega\mu_0}{4\pi k_0^2}\sin\phi[F_{\phi 0}(\rho, z-d) - F_{\phi 0}(\rho, z+d) + F_{\phi 1}(\rho, z+d)] \tag{C.45}$$

where

$$F_{\phi 0}(\rho, z-d) \tag{C.46}$$

$$= \int_0^\infty \left(\frac{\gamma_0}{2}\{J_0(\lambda\rho) + J_2(\lambda\rho)\} + \frac{k_0^2}{2\gamma_0}\{J_0(\lambda\rho) - J_2(\lambda\rho)\} \right) e^{i\gamma_0|z-d|} \lambda d\lambda$$

$$F_{\phi 0}(\rho, z+d) \tag{C.47}$$

$$= \int_0^\infty \left(\frac{\gamma_0}{2}\{J_0(\lambda\rho) + J_2(\lambda\rho)\} + \frac{k_0^2}{2\gamma_0}\{J_0(\lambda\rho) - J_2(\lambda\rho)\} \right) e^{i\gamma_0(z+d)} \lambda d\lambda$$

$$F_{\phi 1}(\rho, z+d) \tag{C.48}$$

$$= \int_0^\infty \left(\frac{\gamma_0}{2}(Q+1)\{J_0(\lambda\rho) + J_2(\lambda\rho)\} - \frac{k_0^2}{2\gamma_0}(P-1)\{J_0(\lambda\rho) - J_2(\lambda\rho)\} \right) e^{i\gamma_0(z+d)} \lambda d\lambda$$

$$E_{0z} = \frac{i\omega\mu_0}{4\pi k_0^2} \cos\phi [F_{z0}(\rho, z-d) - F_{z0}(\rho, z+d) + F_{z1}(\rho, z+d)] \tag{C.49}$$

where

$$F_{z0}(\rho, z-d) = \pm \int_0^\infty J_1(\lambda\rho) e^{i\gamma_0|z-d|} \lambda^2 d\lambda; \begin{cases} z > d \\ 0 \le z \le d \end{cases} \tag{C.50}$$

$$F_{z0}(\rho, z+d) = \int_0^\infty J_1(\lambda\rho) e^{i\gamma_0(z+d)} \lambda^2 d\lambda \tag{C.51}$$

$$F_{z1}(\rho, z+d) = \int_0^\infty (Q+1) J_1(\lambda\rho) e^{i\gamma_0(z+d)} \lambda^2 d\lambda \tag{C.52}$$

$$B_{0\rho} = -\frac{\mu_0}{4\pi} \sin\phi [G_{\rho 0}(\rho, z-d) - G_{\rho 0}(\rho, z+d) + G_{\rho 1}(\rho, z+d)] \tag{C.53}$$

$$B_{0\phi} = -\frac{\mu_0}{4\pi} \cos\phi [G_{\phi 0}(\rho, z-d) - G_{\phi 0}(\rho, z+d) + G_{\phi 1}(\rho, z+d)] \tag{C.54}$$

where

$$G_{\rho 0}(\rho, z-d) = G_{\phi 0}(\rho, z-d) = \pm\int_0^\infty J_0(\lambda\rho)e^{i\gamma_0|z-d|}\lambda d\lambda;\begin{cases} z > d \\ 0 \le z \le d \end{cases} \tag{C.55}$$

$$G_{\rho 0}(\rho, z+d) = G_{\phi 0}(\rho, z+d) = \int_0^\infty J_0(\lambda\rho)e^{i\gamma_0(z+d)}\lambda d\lambda \tag{C.56}$$

$$\left.\begin{matrix} G_{\rho 1}(\rho, z+d) \\ G_{\phi 1}(\rho, z+d) \end{matrix}\right\} \tag{C.57}$$

$$= \int_0^\infty \left(\frac{1}{2}(Q+1)\{J_0(\lambda\rho) \pm J_2(\lambda\rho)\} - \frac{1}{2}(P-1)\{J_0(\lambda\rho) \mp J_2(\lambda\rho)\}\right)e^{i\gamma_0(z+d)}\lambda d\lambda$$

$$B_{0\rho} = \frac{i\mu_0}{4\pi}\sin\phi[G_{z0}(\rho, z-d) - G_{z0}(\rho, z+d) + G_{z1}(\rho, z+d)] \tag{C.58}$$

$$G_{z0}(\rho, z-d) = \int_0^\infty \gamma_0^{-1} J_1(\lambda\rho)e^{i\gamma_0|z-d|}\lambda^2 d\lambda \tag{C.59}$$

$$G_{z0}(\rho, z+d) = \int_0^\infty \gamma_0^{-1} J_1(\lambda\rho)e^{i\gamma_0(z+d)}\lambda^2 d\lambda \tag{C.60}$$

$$G_{z1}(\rho, z+d) = -\int_0^\infty (P-1)\gamma_0^{-1} J_1(\lambda\rho)e^{i\gamma_0(z+d)}\lambda^2 d\lambda \tag{C.61}$$

In these formulas, $F_{m0}(\rho, z\text{-}d)$ and $G_{m0}(\rho, z\text{-}d)$ represent the direct field, $F_{m0}(\rho, z{+}d)$ and $G_{m0}(\rho, z{+}d)$ represent the ideal reflected field, and $F_{m1}(\rho, z{+}d)$ and $G_{m1}(\rho, z{+}d)$ represent the surface wave fields, m=ρ, ϕ, z.

To compute the fields over a 3-layer medium, note that the P and Q represent the negatives of reflection coefficients of magnetic type and electric type between region 0 and 1, respectively. If P and Q are replaced by the negative of reflection coefficients of magnetic type and electric type of 3 layers as

observed in region 0, the field given by the integrals (C.41)-(C.61) will be the complete field of the dipole over a 3-layered medium.

The reflection coefficients of electric (f_{er}) and magnetic (f_{mr}) types of a 3-layered medium can be computed using Snell's law and boundary conditions.

$$f_r = \frac{x_0 - x_2 - i\left[\left(x_0\frac{x_2}{x_1}\right) - x_1\right]\tan\gamma_1 l}{x_0 + x_2 - i\left[\left(x_0\frac{x_2}{x_1}\right) + x_1\right]\tan\gamma_1 l} \tag{C.62}$$

$f_{er}=f_r$ with $x_n = \frac{\gamma_n}{k_n^2}$ and $f_{mr}=f_r$ with $x_n = \gamma_n$; n=0, 1, 2.

The integrals in the functions F and G with subscript 0 apply to the isolated dipole and its perfect image. They are well-known and can be evaluated without approximations. The exact equations are

$$F_{\rho 0}(\rho, z \pm d) = -e^{ik_0 r}\left[\frac{2k_0}{r^2} + \frac{2i}{r^3} + \left(\frac{z \pm d}{r}\right)^2\left(\frac{ik_0^2}{r} - \frac{3k_0}{r^2} - \frac{3i}{r^3}\right)\right] \tag{C.63}$$

$$F_{\phi 0}(\rho, z \pm d) = -e^{ik_0 r}\left(\frac{ik_0^2}{r} - \frac{k_0}{r^2} - \frac{i}{r^3}\right) \tag{C.64}$$

$$F_{z0}(\rho, z \pm d) = -e^{ik_0 r}\left(\frac{\rho}{r}\right)\left(\frac{z \pm d}{r}\right)\left(\frac{k_0^2}{r} + \frac{3ik_0}{r^2} - \frac{3}{r^3}\right) \tag{C.65}$$

$$G_{\rho 0}(\rho, z \pm d) = G_{\phi 0}(\rho, z \pm d) = -e^{ik_0 r}\left(\frac{z \pm d}{r}\right)\left(\frac{ik_0}{r} - \frac{1}{r^2}\right) \tag{C.66}$$

$$G_{z0}(\rho, z \pm d) = -e^{ik_0 r}\left(\frac{\rho}{r}\right)\left(\frac{k_0}{r} + \frac{i}{r^2}\right) \tag{C.67}$$

In these formulas, $r=r_2=[\rho^2+(z+d)^2]^{1/2}$ for the upper signs, $r=r_1=[\rho^2+(z-d)^2]^{1/2}$ for the lower signs.

The integrals that contain P-1 and Q+1 which represent surface wave fields can be approximated assuming the following inequalities.

$$k_0^2 \ll k_1^2 \ll |k_2|^2 \tag{C.68}$$

$$k_0^2 l^2 \ll k_1^2 l^2 \ll 1 \tag{C.69}$$

When the direct, ideal reflected, and surface wave fields are combined, the final formulas for the electromagnetic field components over a 3-layered medium can be obtained as follows.

$$E_{0\rho}(\rho, \phi, z) = \frac{\omega\mu_0}{4\pi k_0}\cos\phi\left[e^{ik_0 r_1}\left\{\frac{2}{r_1^2} + \frac{2i}{k_0 r_1^3} + \left(\frac{z-d}{r_1}\right)^2\left(\frac{ik_0}{r_1} - \frac{3}{r_1^2} - \frac{3i}{k_0 r_1^3}\right)\right\}\right. \tag{C.70}$$

$$- e^{ik_0 r_2}\left\{\frac{2}{r_2^2} + \frac{2i}{k_0 r_2^3} + \left(\frac{z+d}{r_2}\right)^2\left(\frac{ik_0}{r_2} - \frac{3}{r_2^2} - \frac{3i}{k_0 r_2^3}\right)\right\}$$

$$\left. + 2e^{ik_0 r_2}\left\{\varepsilon\left(\frac{z+d}{r_2}\right)\left(\frac{ik_0}{r_2} - \frac{1}{r_2^2}\right) - \varepsilon^2\left[\frac{ik_0}{r_2} - \frac{1}{r_2^2} - \frac{i}{k_0 r_2^3} - k_0^2\varepsilon\left(\frac{r_2}{\rho}\right)\left(\frac{\pi}{k_0 r_2}\right)^{\frac{1}{2}} e^{-iP_2}\Im(P_2)\right]\right\}\right]$$

$$E_{0\phi}(\rho,\phi,z) = -\frac{\omega\mu_0}{4\pi k_0}\sin\phi\left[e^{ik_0r_1}\left(\frac{ik_0}{r_1}-\frac{1}{r_1^2}-\frac{i}{k_0r_1^3}\right)-e^{ik_0r_2}\left(\frac{ik_0}{r_2}-\frac{1}{r_2^2}-\frac{i}{k_0r_2^3}\right)\right. \tag{C.71}$$

$$+2e^{ik_0r_2}\left\{\varepsilon\left(\frac{z+d}{r_2}\right)\left(\frac{ik_0}{r_2}-\frac{1}{r_2^2}\right)\right.$$

$$\left.\left.-\varepsilon^2\left[\frac{2}{r_2^2}+\frac{2i}{k_0r_2^3}+\left(\frac{z+d}{r_2}\right)^2\left(\frac{ik_0}{r_2}-\frac{3}{r_2^2}-\frac{3i}{k_0r_2^3}\right)+ik_0\varepsilon\left(\frac{r_2^2}{\rho^3}\right)\left(\frac{\pi}{k_0r_2}\right)^{\frac{1}{2}}e^{-iP_2}\Im(P_2)\right]\right\}\right]$$

$$E_{0z}(\rho,\phi,z) = -\frac{\omega\mu_0}{4\pi k_0}\cos\phi\left[e^{ik_0r_1}\left(\frac{\rho}{r_1}\right)\left(\frac{z-d}{r_1}\right)\left(\frac{ik_0}{r_1}-\frac{3}{r_1^2}-\frac{3i}{k_0r_1^3}\right)\right. \tag{C.72}$$

$$-e^{ik_0r_2}\left(\frac{\rho}{r_2}\right)\left(\frac{z+d}{r_2}\right)\left(\frac{ik_0}{r_2}-\frac{3}{r_2^2}-\frac{3i}{k_0r_2^3}\right)$$

$$\left.+2\varepsilon e^{ik_0r_2}\left\{\left(\frac{\rho}{r_2}\right)\left(\frac{ik_0}{r_2}-\frac{1}{r_2^2}\right)-k_0^2\varepsilon\left(\frac{\pi}{k_0r_2}\right)^{\frac{1}{2}}e^{-iP_2}\Im(P_2)\right\}\right]$$

$$B_{0\rho}(\rho,\phi,z) = \frac{\mu_0}{4\pi}\sin\phi\left[e^{ik_0r_1}\left(\frac{z-d}{r_1}\right)\left(\frac{ik_0}{r_1}-\frac{1}{r_1^2}\right)-e^{ik_0r_2}\left(\frac{z+d}{r_2}\right)\left(\frac{ik_0}{r_2}-\frac{1}{r_2^2}\right)\right. \tag{C.73}$$

$$\left.+2\varepsilon e^{ik_0r_2}\left\{\frac{2}{r_2^2}+\frac{2i}{k_0r_2^3}+\left(\frac{z+d}{r_2}\right)^2\left(\frac{ik_0}{r_2}-\frac{3}{r_2^2}-\frac{3i}{k_0r_2^3}\right)+ik_0\varepsilon\left(\frac{r_2^2}{\rho^3}\right)\left(\frac{\pi}{k_0r_2}\right)^{\frac{1}{2}}e^{-iP_2}\Im(P_2)\right\}\right]$$

$$B_{0\phi}(\rho, \phi, z) = \frac{\mu_0}{4\pi}\cos\phi\left[e^{ik_0r_1}\left(\frac{z-d}{r_1}\right)\left(\frac{ik_0}{r_1}-\frac{1}{r_1^2}\right)-e^{ik_0r_2}\left(\frac{z+d}{r_2}\right)\left(\frac{ik_0}{r_2}-\frac{1}{r_2^2}\right)\right. \tag{C.74}$$

$$\left.+2\varepsilon e^{ik_0r_2}\left\{\frac{ik_0}{r_2}-\frac{1}{r_2^2}-\frac{i}{k_0r_2^3}-k_0^2\varepsilon\left(\frac{r_2}{\rho}\right)\left(\frac{\pi}{k_0r_2}\right)^{\frac{1}{2}}e^{-iP_2}\Im(P_2)\right\}\right]$$

$$B_{0z}(\rho, \phi, z) = -\frac{\mu_0}{4\pi}\sin\phi\left[e^{ik_0r_1}\left(\frac{\rho}{r_1}\right)\left(\frac{ik_0}{r_1}-\frac{1}{r_1^2}\right)-e^{ik_0r_2}\left(\frac{\rho}{r_2}\right)\left(\frac{ik_0}{r_2}-\frac{1}{r_2^2}\right)+2e^{ik_0r_2}\right. \tag{C.75}$$

$$\left\{\left(\varepsilon\left(\frac{r_2}{\rho}\right)\left(\frac{z+d}{r_2}\right)\right)\left(\frac{ik_0}{r_2}-\frac{3}{r_2^2}-\frac{3i}{k_0r_2^3}\right)\right.$$

$$\left.\left.-\varepsilon^2\left(\frac{\rho}{r_2}\right)\left[\frac{1}{r_2^2}+\frac{3i}{k_0r_2^3}-\frac{3}{k_0^2r_2^4}+\left(\frac{z+d}{r_2}\right)^2\left(\frac{ik_0}{r_2}-\frac{6}{r_2^2}-\frac{15i}{k_0r_2^3}\right)\right]\right\}\right]$$

In these equations,

$$\varepsilon = \frac{\left(\frac{k_0}{k_2}\right)-ik_0l}{1-\frac{ik_1^2}{k_2}} \tag{C.76}$$

$$P_2 = \frac{k_0r_2}{2}\left(\frac{\varepsilon r_2+z+d}{\rho}\right) \tag{C.77}$$

$$\Im(P_2) = \frac{1}{2}(1+i)-\int_0^{P_2}\frac{e^{it}}{\sqrt{2\pi t}}dt \tag{C.78}$$

The integral in $\Im(P_2)$ is the well-known Fresnel integral.

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